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# MEMORY SYSTEMS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

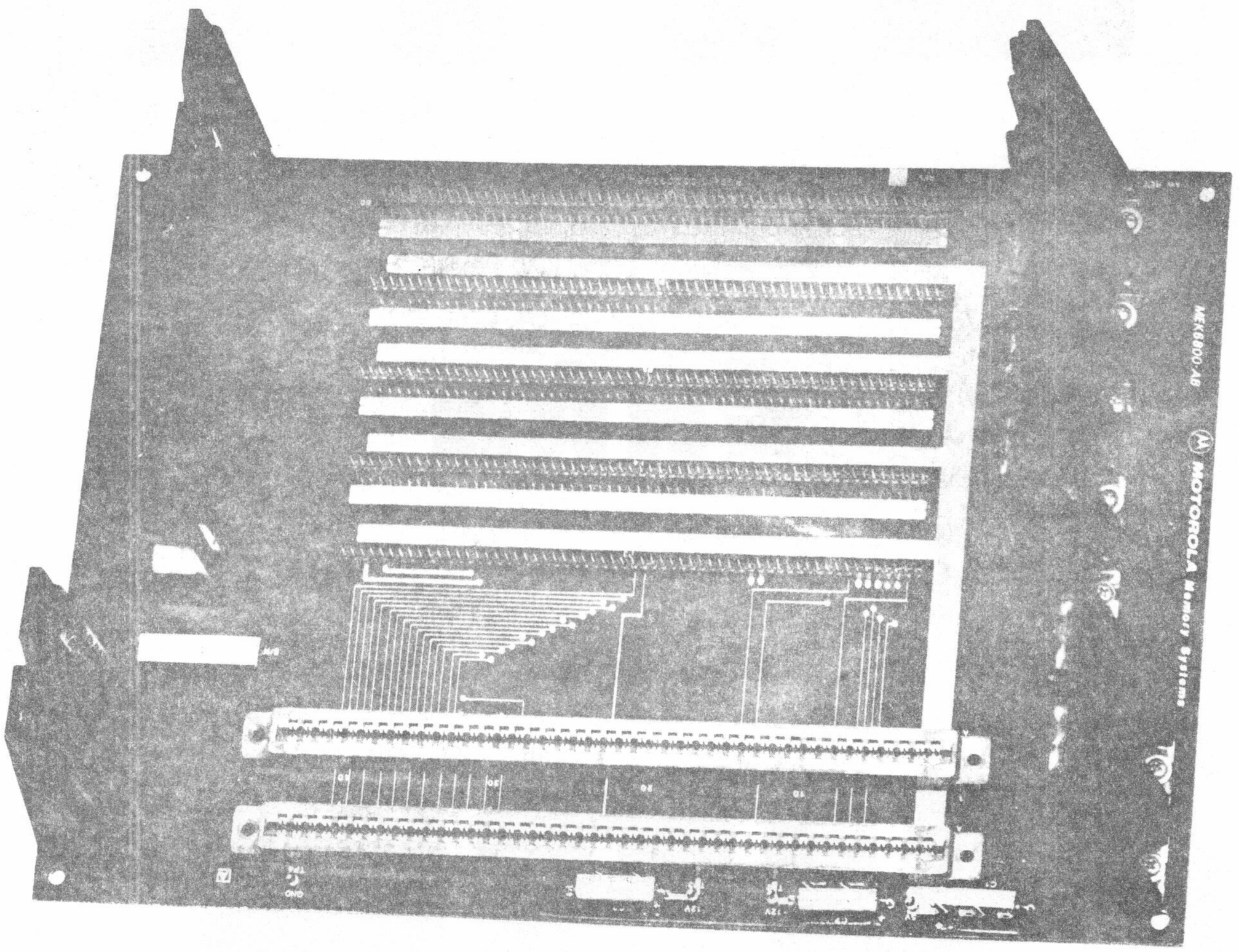
$88

# MEK6800AB

## Advance Information

### ADAPTER/MOTHERBOARD

The MEK6800AB is an Adapter/Motherboard designed to allow the MEK6800D2 Evaluation Kit and the MMS68104 dynamic memory module to be used with the newer MOKEP (Motorola Kit Expansion Products) series. The MEK6800AB requires a minimal assembly to attach the freestanding card guides. All connectors and capacitors are installed at the factory.




- Five MOKEP Compatible (60-pin) Connectors
- Two MEK6800D2/MMS68104 Compatible (86-pin) Connectors
- Filter Capacitors Installed for the +12, −12, and +5 V Supplies
- Freestanding Card Guides for Seven Positions

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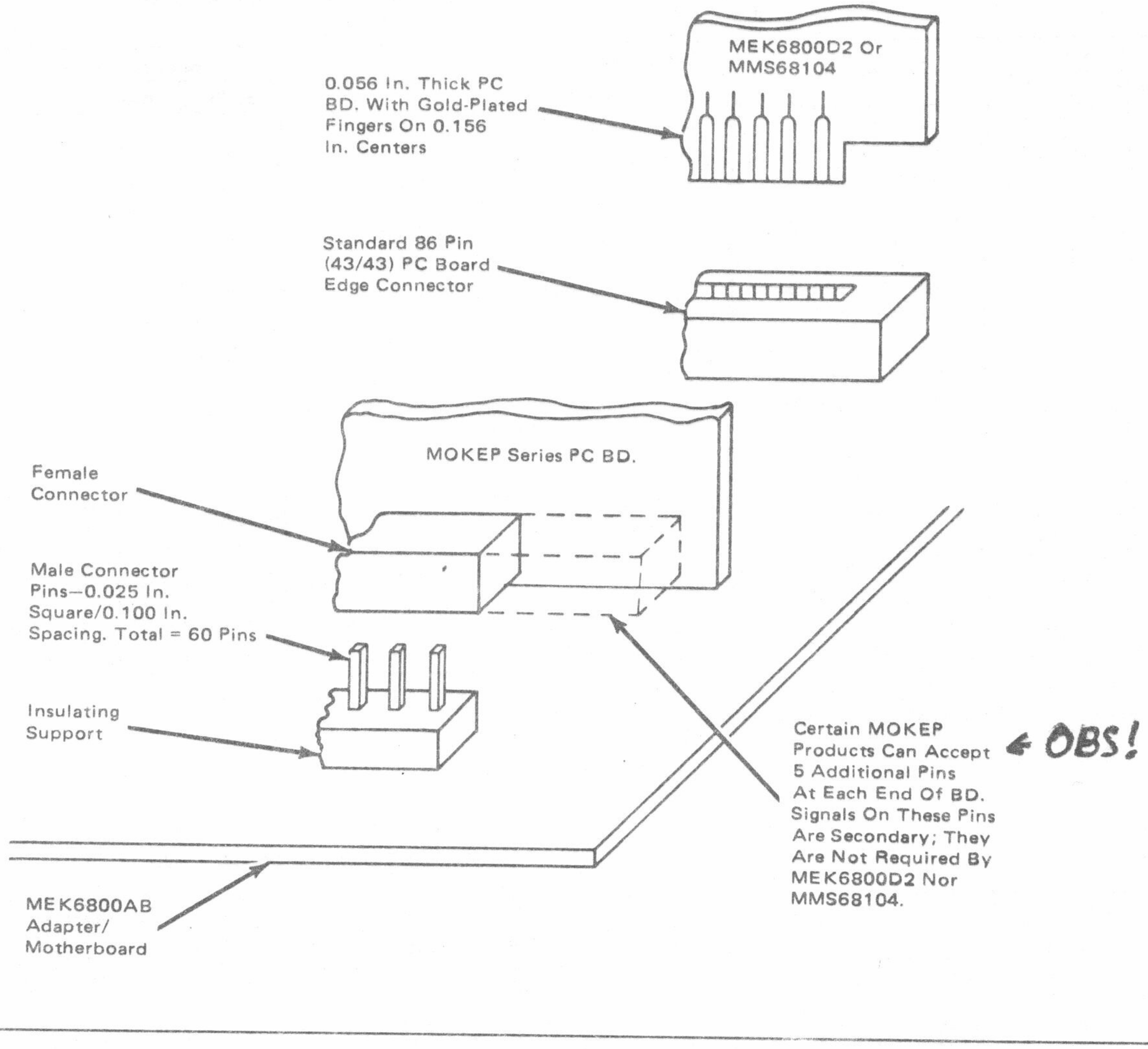
FIGURE 2 – CONNECTOR DETAILS




## MODIFICATIONS REQUIRED FOR MEK6800D2 EXPANSION

As supplied, the MEK6800D2 has no Address/Data Buffers required to drive the bus. Prior to utilizing the MEK6800D2 with the MEK6800AB, it is necessary to install five buffer packages and one gate. The device types and locations are:

U1 – MC8T97
U2 – MC8T97
U3 – MC8T97
U4 – MC8T28
U5 – MC8T28
U7 – MC7430 or 74LS30

It should be noted that the D2 manual specifies MC8T26 Transmitter/Receivers for locations U4 and U5. These are inverting devices, whereas the MC8T28 is a non-inverting product with the same pinouts. All MOKEP series modules are designed to operate with True Data on the bus. If these products are to be used, and MC8T26s have previously been installed, it is necessary to replace the MC8T26s with MC8T28s.

It is also necessary to route VMA to pin F of the MEK6800D2 connector. Recommended ways of doing this are contained in subsequent sections dealing with Memory Map Expansion (Figure 5) and MEK68104 usage (Figure 10).

An expanded system often creates more noise than is prevalent with the two-board D2 configuration. It is, therefore, recommended that 10K pull-up resistors be connected to the $\overline{\text{Hold1}}$ and $\overline{\text{Hold2}}$ inputs of the MC6871B clock. A convenient means of accomplishing this is to locate the two feed-through holes closest to pin 1

## TABLE 2 – INTERCONNECTION REFERENCED TO 60-PIN CONNECTOR

| Connector | | Signal | Connector | | Signal | Connector | | Signal |
|---|---|---|---|---|---|---|---|---|
| 60-Pin | 86-Pin | | 60-Pin | 86-Pin | | 60-Pin | 86-Pin | |
| 1 | Various | Gnd | 21 | 19** | ROP0 (ROM Pg 0) | 41 | 35 | A11 |
| 2 | J | E (Clock Phase 2) | 22 | W** | ROP1 (ROM Pg 1) | 42 | 34 | A12 |
| 3 | – | +5V Standby | 23 | $\overline{A}$** | ROP2 (ROM Pg 2) | 43 | $\overline{N}$ | A13 |
| 4 | VAR | +5V | 24 | 25** | RAP0 (RAM Pg 0) | 44 | $\overline{M}$ | A14 |
| 5 | – | BS (Bus Status)* | 25 | $\overline{C}$** | RAP1 (RAM Pg 1) | 45 | 33 | A15 |
| 6 | – | Open | 26 | 26** | RAP2 (RAM Pg 2) | 46 | Various | Gnd |
| 7 | – | $\overline{BReq}$ ($\overline{Bus\ Request}$)* | 27 | $\overline{D}$** | I/O1 ($8000-$807F) | 47 | Various | Gnd |
| 8 | R | Mem Ready | 28 | 27** | I/O2 ($8080-80FF) | 48 | 31 | D0 |
| 9 | F | VMA | 29 | 23 | $\overline{Active}$ | 49 | 29 | D1 |
| 10 | P | BA (Bus Available) | 30 | 40 | A0 | 50 | $\overline{K}$ | D2 |
| 11 | 6 | R/$\overline{W}$ (Read/$\overline{Write}$) | 31 | $\overline{V}$ | A1 | 51 | $\overline{H}$ | D3 |
| 12 | – | Gnd | 32 | $\overline{U}$ | A2 | 52 | 32 | D4 |
| 13 | 5 | $\overline{Reset}$ | 33 | 39 | A3 | 53 | 30 | D5 |
| 14 | E | $\overline{NMI}$ | 34 | 38 | A4 | 54 | $\overline{L}$ | D6 |
| 15 | D | $\overline{IRQ}$ | 35 | $\overline{T}$ | A5 | 55 | $\overline{J}$ | D7 |
| 16 | 4 | $\overline{Halt}$ | 36 | $\overline{S}$ | A6 | 56 | T,16 | +12V |
| 17 | – | $\overline{FIRQ}$* | 37 | 37 | A7 | 57 | Various | Gnd |
| 18 | – | $Q_{out}$ (Clock)* | 38 | 36 | A8 | 58 | M,11 | –12V |
| 19 | – | Gnd | 39 | $\overline{R}$ | A9 | 59 | Various | +5V |
| 20 | Various | Key Slot | 40 | $\overline{P}$ | A10 | 60 | Various | Gnd |

*Future signal allocation for MC6809

**Connection to be made by user if function is generated on D2 Kit.

## TABLE 3 – INTERCONNECTION REFERENCED TO 86-PIN CONNECTOR

| Connector | | Signal | Connector | | Signal | Connector | | Signal | Connector | | Signal |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 86-Pin | 60-Pin | | 86-Pin | 60-Pin | | 86-Pin | 60-Pin | | 86-Pin | 60-Pin | |
| 1 | 4,59 | +5V | A | 4,59 | +5V | 23 | 29 | $\overline{Active}$ | $\overline{A}$* | 23 | ROP2 |
| 2 | 4,59 | +5V | B | 4,59 | +5V | 24 | – | – | $\overline{B}$ | – | – |
| 3 | 4,59 | +5V | C | 4,59 | +5V | 25 | – | –5V | $\overline{C}$* | 24 | RAP0 |
| 4 | 16 | $\overline{Halt}$ | D | 15 | $\overline{IRQ}$ | 26* | 25 | RAP1 | $\overline{D}$* | 26 | RAP2 |
| 5 | 13 | $\overline{Reset}$ | E | 14 | $\overline{NMI}$ | 27* | 27 | I/O1 | $\overline{E}$ | – | – |
| 6 | 11 | R/$\overline{W}$ | F | 9 | VMA | 28* | 28 | I/O2 | $\overline{F}$ | – | – |
| 7 | – | – | H | VAR | ±12V Gnd | 29 | 49 | D1 | $\overline{H}$ | 51 | D3 |
| 8 | VAR | ±12V Gnd | J | 2 | E | 30 | 53 | D5 | $\overline{J}$ | 55 | D7 |
| 9 | VAR | ±12V Gnd | K | VAR | ±12V Gnd | 31 | 48 | D0 | $\overline{K}$ | 50 | D2 |
| 10 | – | – | L | – | Mem Clk | 32 | 52 | D4 | $\overline{L}$ | 54 | D6 |
| 11 | 58 | –12V | M | 58 | –12V | 33 | 45 | A15 | $\overline{M}$ | 44 | A14 |
| 12 | – | $\overline{Ref\ Req}$ | N | – | TSC | 34 | 42 | A12 | $\overline{N}$ | 43 | A13 |
| 13 | – | $\overline{Ref\ Gnt}$ | P | 10 | BA | 35 | 41 | A11 | $\overline{P}$ | 40 | A10 |
| 14 | – | – | R | – | – | 36 | 38 | A8 | $\overline{R}$ | 39 | A9 |
| 15 | – | – | S | – | – | 37 | 37 | A7 | $\overline{S}$ | 36 | A6 |
| 16 | 56 | +12V | T | 56 | +12V | 38 | 34 | A4 | $\overline{T}$ | 35 | A5 |
| 17 | – | – | U | – | – | 39 | 39 | A3 | $\overline{U}$ | 32 | A2 |
| 18 | – | – | V | – | – | 40 | 30 | A0 | $\overline{V}$ | 31 | A1 |
| 19* | 21 | ROP0 | W* | 22 | ROP1 | 41 | VAR | Gnd | $\overline{W}$ | VAR | Gnd |
| 20 | – | $\overline{2/3}$ | X | – | $\overline{H1}$ | 42 | VAR | Gnd | $\overline{X}$ | VAR | Gnd |
| 21 | – | $\overline{4/5}$ | Y | – | $\overline{H2}$ | 43 | VAR | Gnd | $\overline{Y}$ | VAR | Gnd |
| 22 | – | $\overline{RAM}$ | Z | – | – | | | | | | |

*Connection to be made by user if function is generated on D2 Kit.

of U11. Connect two 10k resistors between these feed-through holes and the one located at the end of the $V_{CC}$ trace approximately 1¼ inches to the left. (This $V_{CC}$ trace connects to pin 22 of U20.)

## MEK6800D2 MEMORY MAP DEFINITION

The MEK68AB is designed to allow the D2 to be easily expanded to form a powerful microcomputer system. In order to utilize the capabilities of the MC6800, it is necessary to make certain modifications to the D2. One requirement involves re-definition of the D2 memory map. The extent of these modifications depends upon the intended use of the system.

Three techniques for memory map re-definition are illustrated in the ensuing paragraphs. The examples given are believed to be the ones most useful for a general purpose microcomputer unit. They can be implemented independently, if desired. Perhaps more importantly, the techniques can be expanded to other areas of the memory map.

One of the recommended memory map modifications consists of making the area from $0000 through $7FFF available for external User RAM. This involves moving the MCM6810s (U14, U16, U18, & U19) and the ROM/EPROM socket (U12) to new locations in the memory map. The recommended new location for the ROM/EPROM socket is $E000, which is the same location as the JBUG monitor ROM (U8). The exact details of this modification depends on the intended usage, and examples are contained in the section of this data sheet dealing with Memory Paging. In any event, it is necessary to cut the trace at pin 7 of U11. This de-activates the $\overline{PROM1}$ signal which would normally turn off the data bus (via U7) for addresses between $6000 and $7FFF.

The On-Board User RAM can be used effectively as a User Stack in an expanded system. The recommended starting location for this Stack is $8200. With all sockets filled, this creates a User Stack extending from $8200 through $83FF. Since the MC6800 creates stacks extending downward in memory, the locations from $8300 through $83FF should be filled if only the two User RAM 6810s supplied with the D2 are available.

Implementation of this stack involves cutting the trace at pin 4 of U11, and configuring a decoding circuit as shown in Figure 3. Note that the new $\overline{RAM}$ signal disables the data bus for addresses between $8200 and $87FF. This is done to allow a system controller EPROM to be used for U12, or for 1024 bytes of RAM to be located in the wire-wrap area.

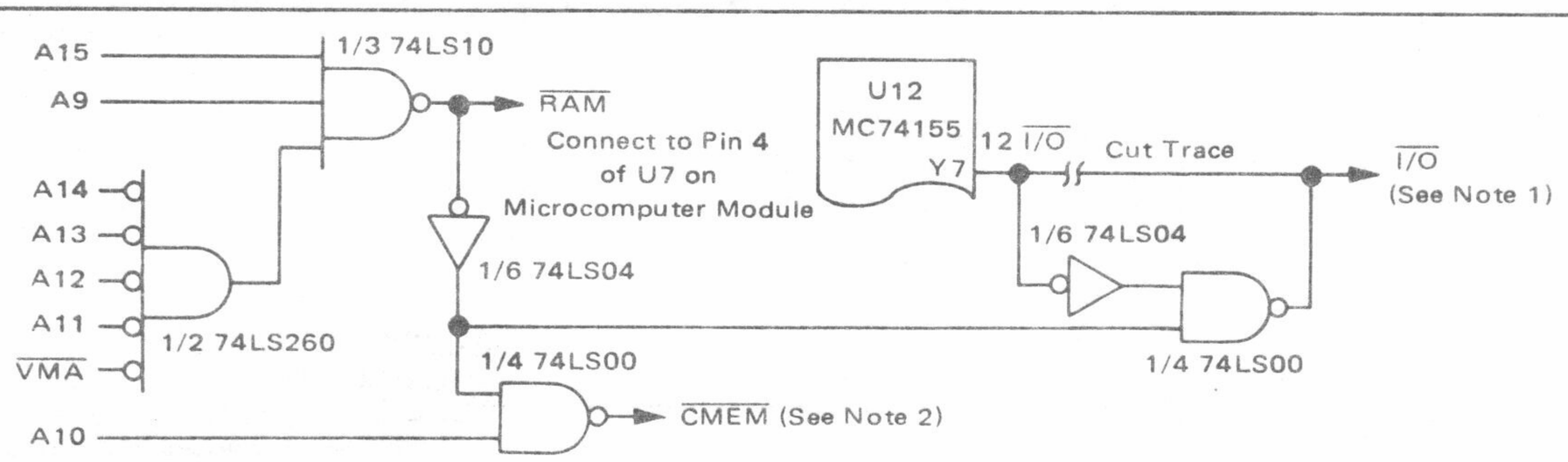
The modifications made to the memory map thus far are depicted in Figure 4. The technique used has been to implement On-Board decoding in conjunction with modification of the signals driving U7. This results in the D2 responding to an external device located from $0000 through $7FFF.

A second technique useful in modifying the memory map involves disabling the MC74155 decoder (via the $\overline{Strobe}$ inputs) for certain addresses. An important advantage of this method is that the address decoding can be accomplished on an external module. Both the MEK68R2 CRT Interface Module and the MEK68EP EPROM Programmer Module contain circuitry to be used with this technique. The recommended modifications are shown in Figure 5. Note that no additional I.C.'s are needed to implement these changes, since two unused NAND gates are included on the D2.

The modification of Figure 5 also provides a VMA signal at pin F of the 86-pin connector. This is a requirement for most modules designed for use with the AB/D2 combination. Thus, the modification is recommended for all systems.

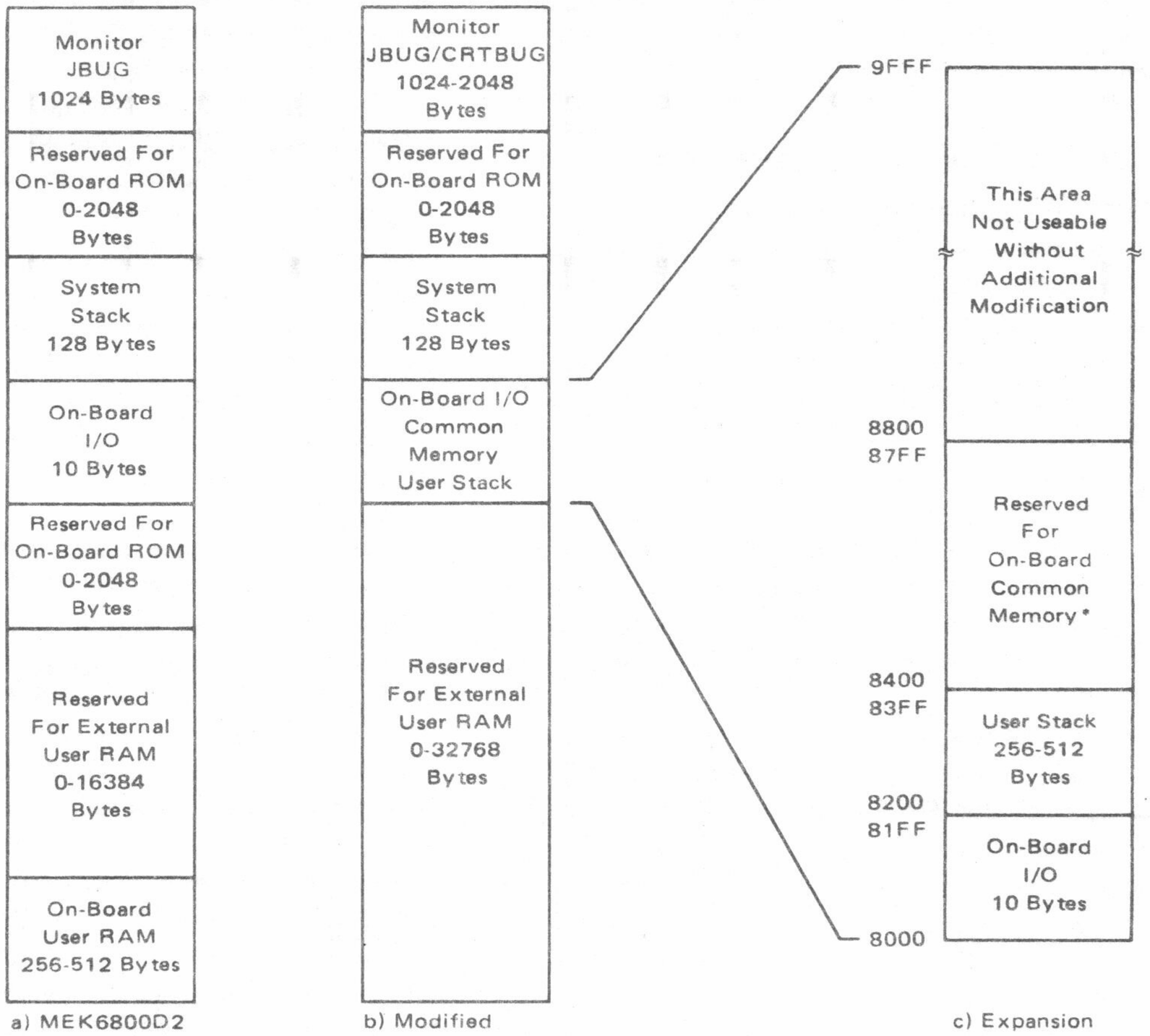
The MEK68R2 CRT Interface Module forces the $\overline{Active}$ line low (via an open collector driver) for addresses between $8040 and $9FFF. This results in the $\overline{I/O}$ output (pin 12) of the MC74155 being low only for addresses between $8000 and $803F. If the MEK68R2 is not used in the system, a decoding circuit such as those shown in Figure 6 should be implemented in the Wire-Wrap area.

**FIGURE 3 – IMPLEMENTATION OF USER STACK**




Note 1: This connection not required if an MEK68R2 is used or if on-board I/O is deselected via circuitry of Figure 5.
Note 2: This signal required only if 1024 Byte RAM is added to wire-wrap area or if user supplied system controller EPROM is to be used in position U12.

**FIGURE 4 – MEMORY MAP MODIFICATIONS**




* As used here, Common Memory refers to ROM or RAM which is accessible on any page of the memory map. With modifications shown thus far, all memory and I/O is "Common" Memory.

**FIGURE 5 – IMPLEMENTATION OF $\overline{\text{ACTIVE}}$**

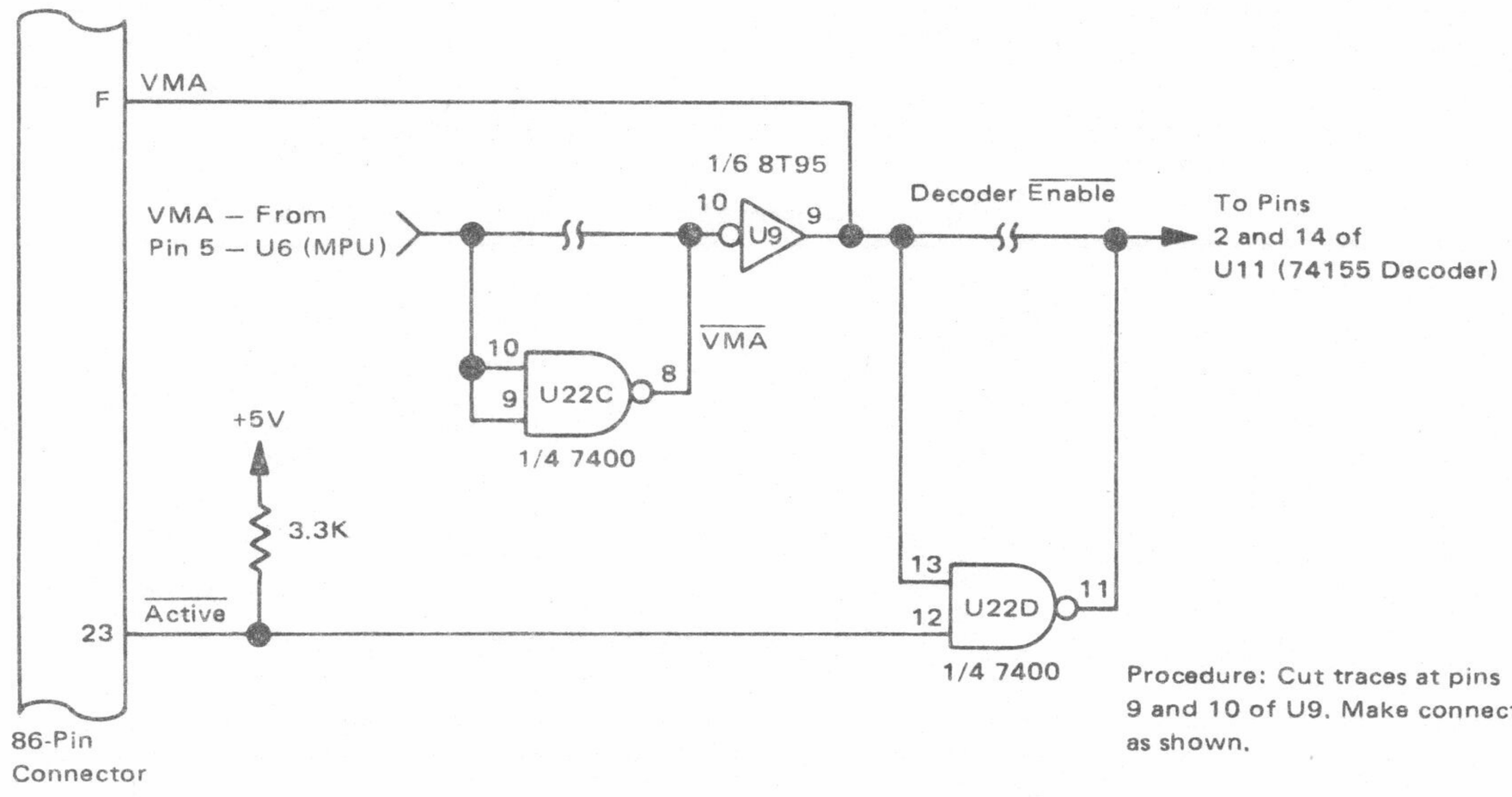
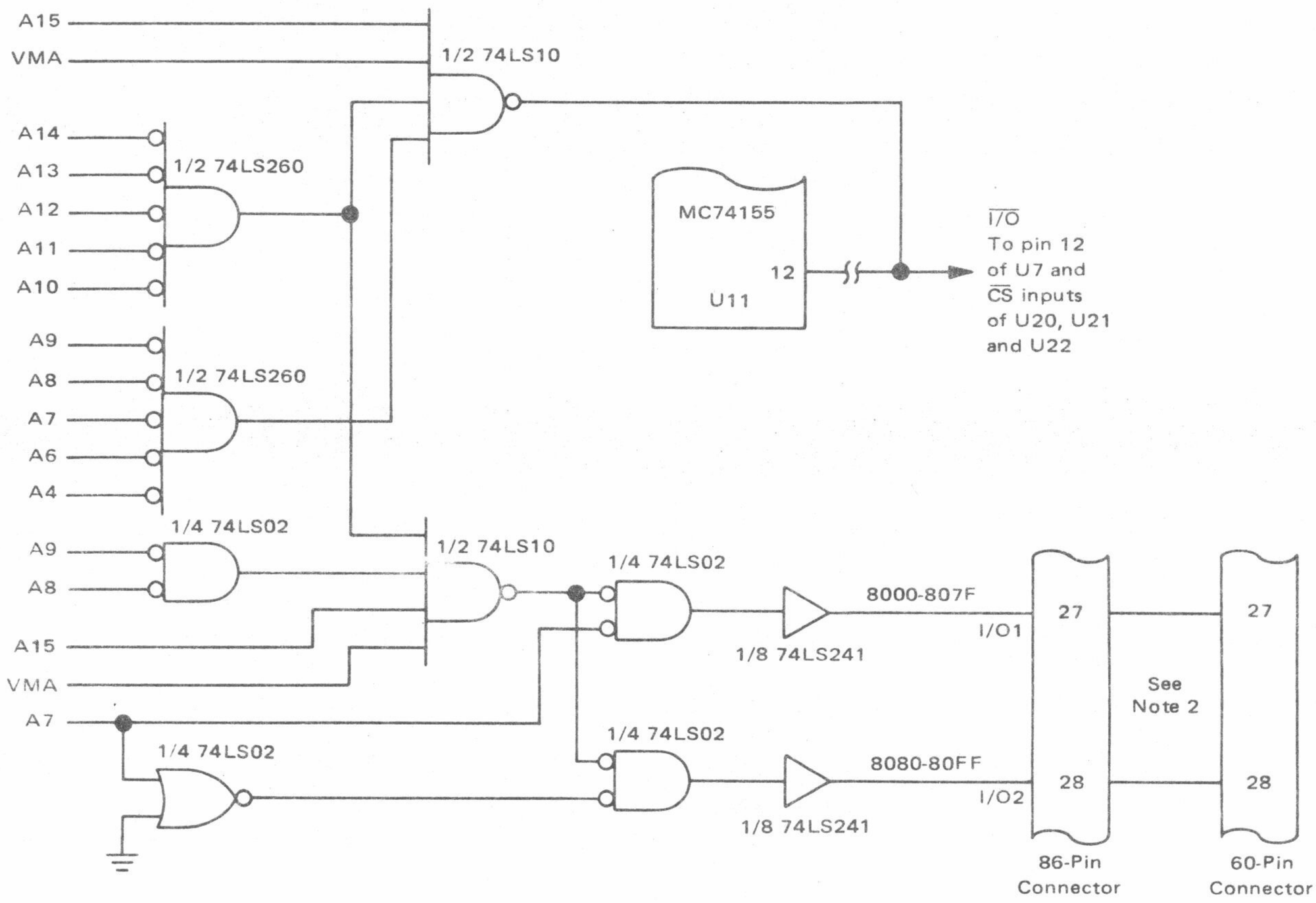


FIGURE 6 – ON-BOARD I/O DECODING CIRCUITRY




NOTES:

1) Circuitry associated with I/O1 and I/O2 required only if MEK68R2 is not used and module requiring partially decoded signals (e.g., MEK68IO, MEK68EP) is used.

2) Point-to-point wiring to be implemented by user if I/O1 and I/O2 is generated on MEK6800D2.

A third technique for modifying the memory map involves memory paging. A convenient technique for accomplishing this is to utilize Port A of the User PIA (U20). The MEK6800AB is not designed to support this, so it is necessary to utilize point-to-point wiring on the backplane to take full advantage of the technique. The memory modules (including the ROM/RAM card) do support both ROM and RAM paging, as does the EPROM programmer.

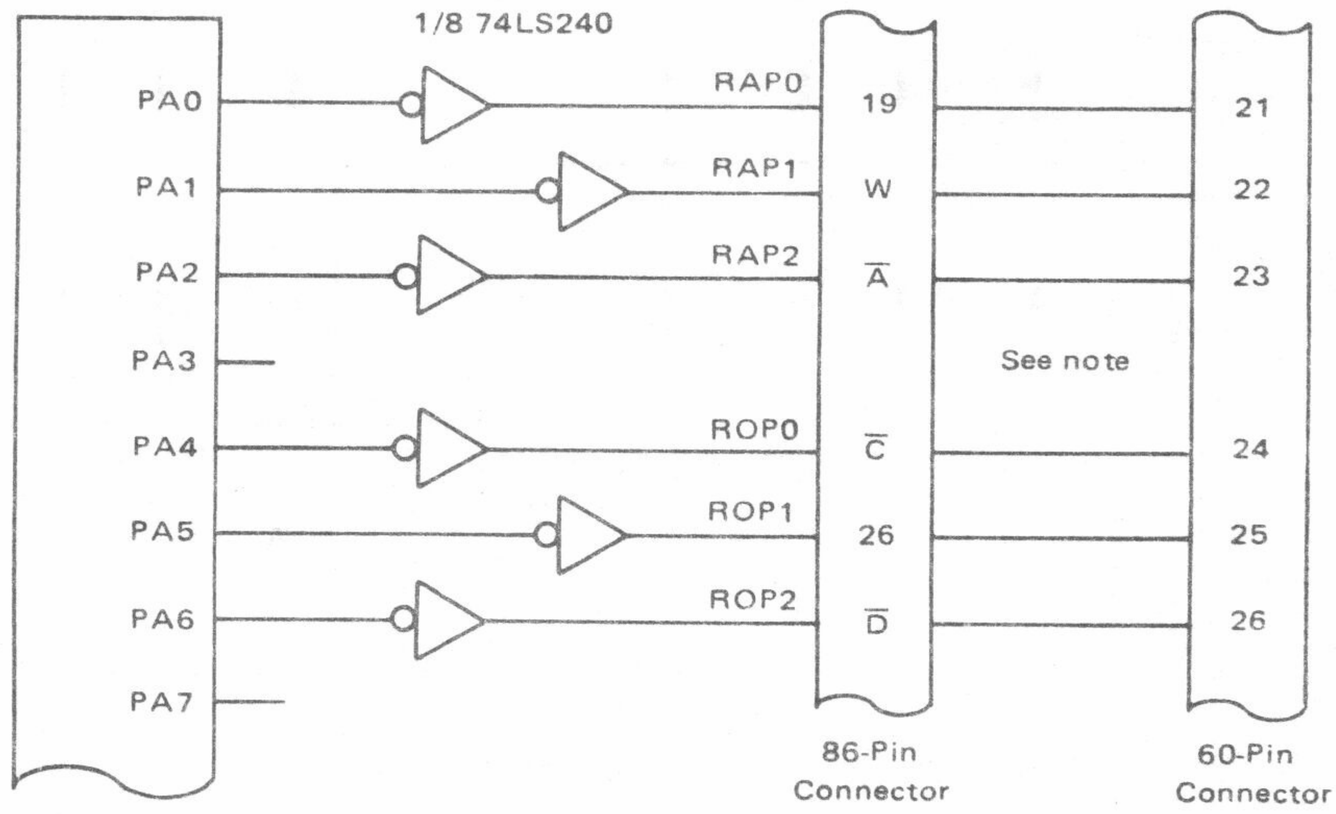
As shown in Figure 7, one port of the PIA and six inverting buffers are required to implement the memory paging technique used by the MOKEP series. Note that System Reset converts the PIA ports to inputs. The internal pullup resistors incorporated in port A insure that PA0 – PA7 assume logic one levels until the Data Direction Register of the PIA is complemented. Thus, the System Reset automatically causes ROM and RAM pages to be initialized to zero.

As an example of the memory paging technique, it may be desirable to use both JBUG and CRTBUG in the same system. This can be done by locating JBUG on Page Zero and CRTBUG on Pages 1-3. Figure 8 depicts one technique for accomplishing this.

When the memory paging technique is used for monitor ROMs, it is necessary to develop a program routine in some common memory area to allow switching of monitors under program control. The basic requirement of this routine is that it must change the data register of the User PIA, then Jump to the start of the appropriate subroutine in the monitor selected. Embellishments of the monitor switching routine can include the capability of monitor call and return, stack control, interrupt vector control, etc., to serve the needs of a particular system.

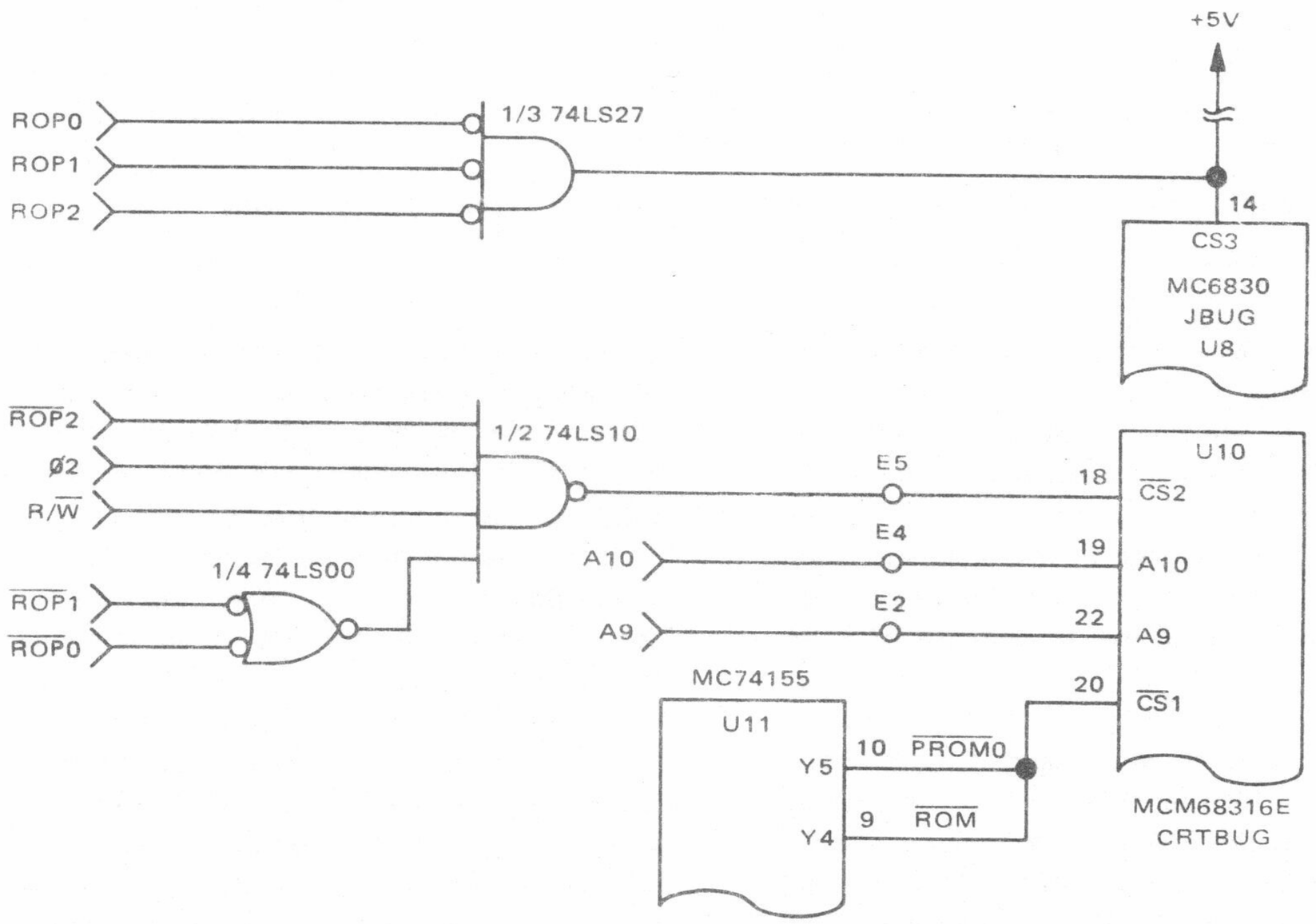
The Memory Map of Figure 9 will result if all the modifications discussed heretofore are incorporated. Further changes can be implemented by the user via one or more

FIGURE 7 – IMPLEMENTATION OF MEMORY PAGING




NOTE: Point-to-point wiring on backplane (user implemented) is required for this function

FIGURE 8 – EXAMPLE OF ROM PAGING



of the techniques noted. For most systems, however, the Memory Map of Figure 9 will prove sufficient.

## APPLICATION OF THE MMS68104 MEMORY MODULE TO THE MEK6800D2 KIT

There are two steps involved in interfacing the 68104 memory to the D2 kit. One of these is to insure that the required memory space is available. This can be done through utilization of one of the techniques described previously. It can also be accomplished by merely unplugging the MCM6810 User RAMs, cutting the trace to pin 4 of U7, and connecting U7 – pin 4 to $V_{CC}$.

The second step is to provide a synchronization circuit for the Refresh Request/Refresh Grant signals. The required circuitry is depicted in Figure 10. Note that a time delay Reset signal is included in the schematic. Without this precaution, it would be impossible for the system to power up with both the Refresh Request and Refresh Grant signals active. This would cause the system to lock into an inoperative state. The circuitry as shown prevents this from occurring.

**FIGURE 9 – REVISED MEK6800D2 MEMORY MAP**

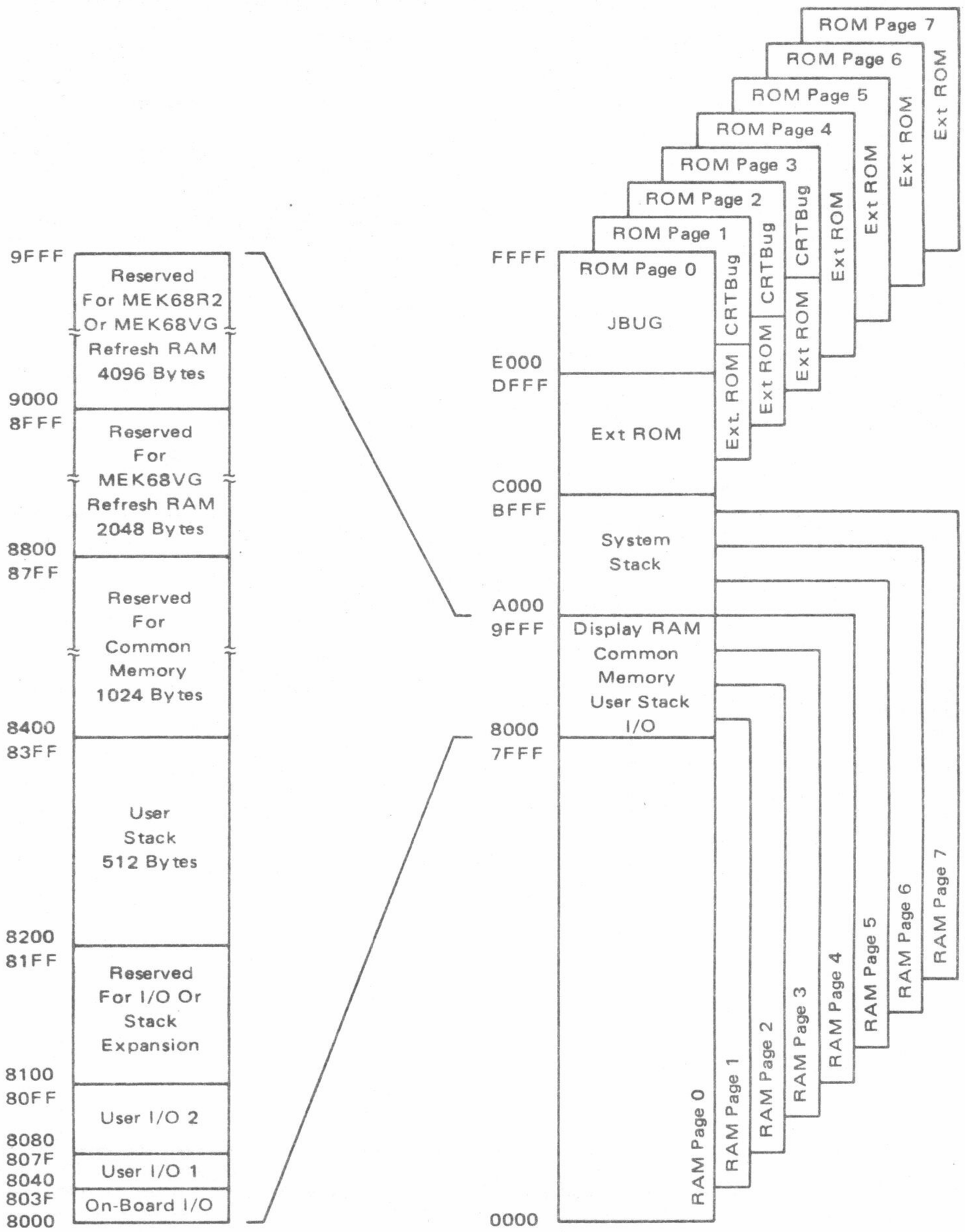
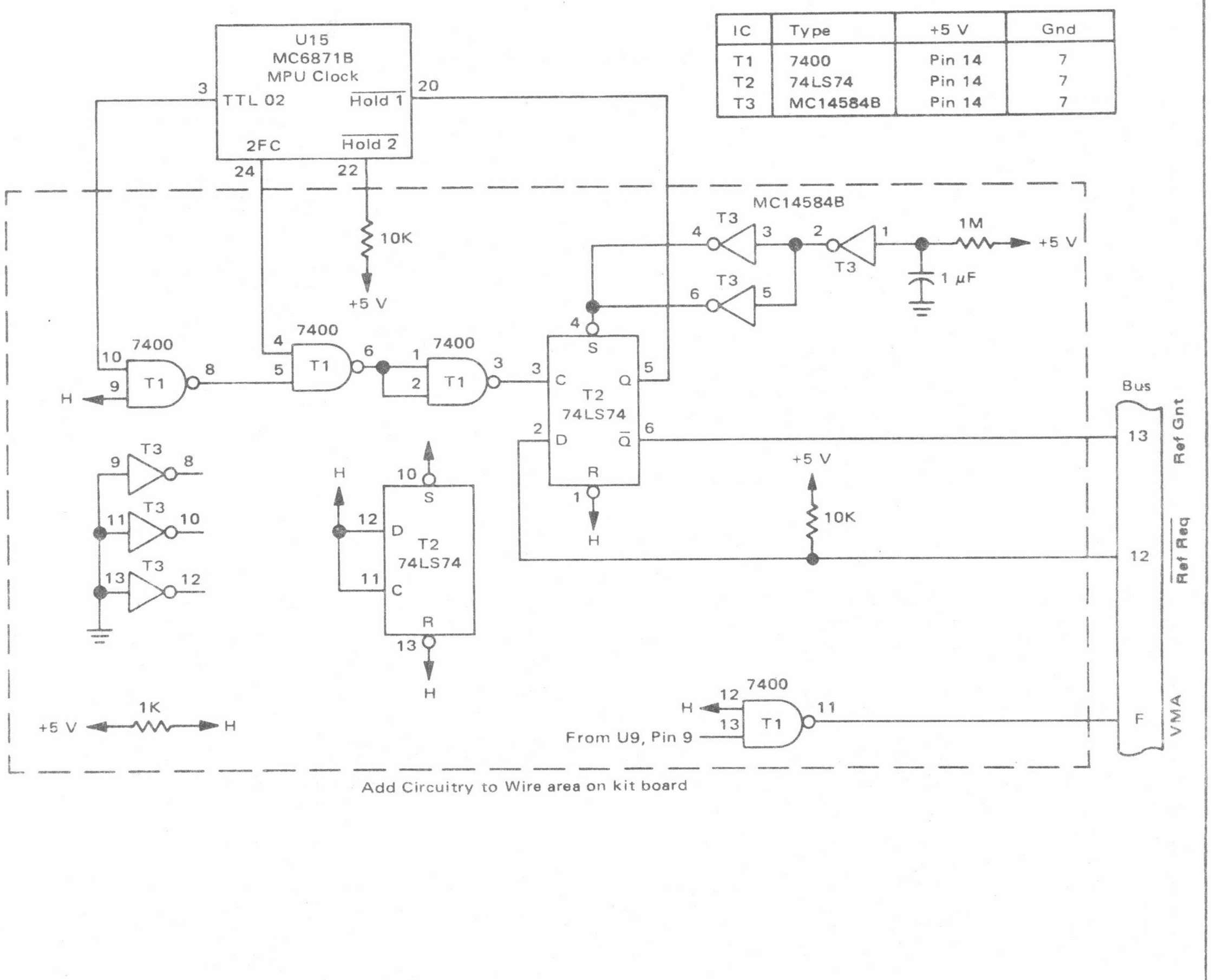


FIGURE 10 – APPLICATION OF THE MMS68104 BOARD TO THE D-2 KIT




Add Circuitry to Wire area on kit board

MOTOROLA

# MEMORY SYSTEMS

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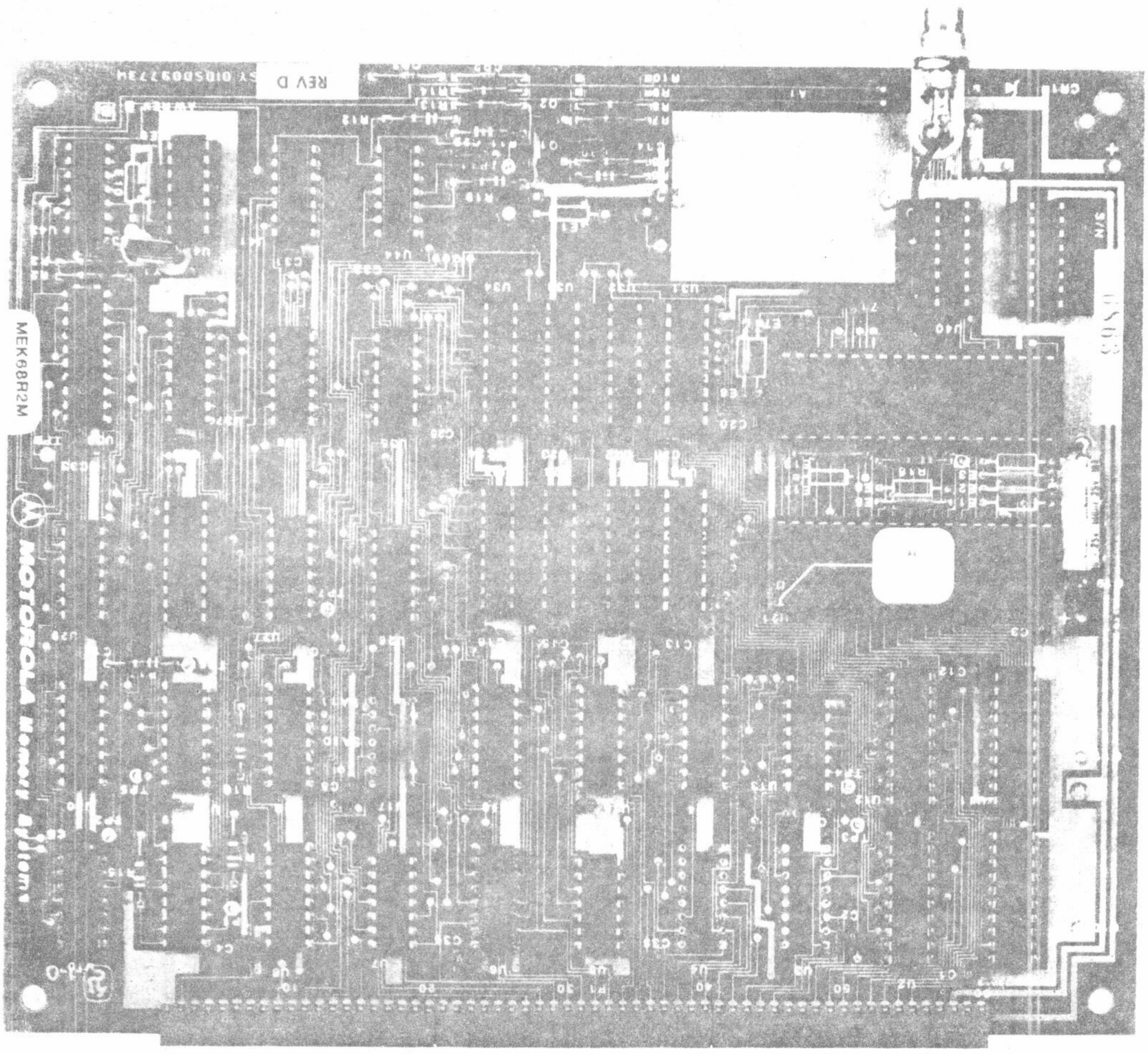
2.

**MEK68R2**
**MEK68R2M**
$200

## Advance Information

## PROGRAMMABLE CRT INTERFACE

The MEK68R2/MEK68R2M CRT Interface Modules are designed to be used in conjunction with other products in the MOKEP (Motorola Kit Expansion Products) family to form a powerful microcomputer system. The MEK68R2 is designed specifically for use with the MEK6800D2 microcomputer module and MEK6800AB Adapter/Motherboard. The MEK68R2M is to be used with an MEK6802D3 microcomputer module and an MEK68MB series motherboard. Both units feature software programmable line and character format, upper and lowercase 5 × 7 matrix display, and up to 4K bytes of Screen Refresh Memory. Either model provides an interface to an ASCII keyboard along with provisions for a light pen input.




- Interfaces to B/W CRT Monitor (or modified TV set) and ASCII Encoded Keyboard
- Supplied with 1K Byte of Screen Refresh RAM-Expandable to 4K
- 16 × 32, 16 × 64, 20 × 80, or User Defined Formats

MOKEP is a trademark of Motorola Inc.

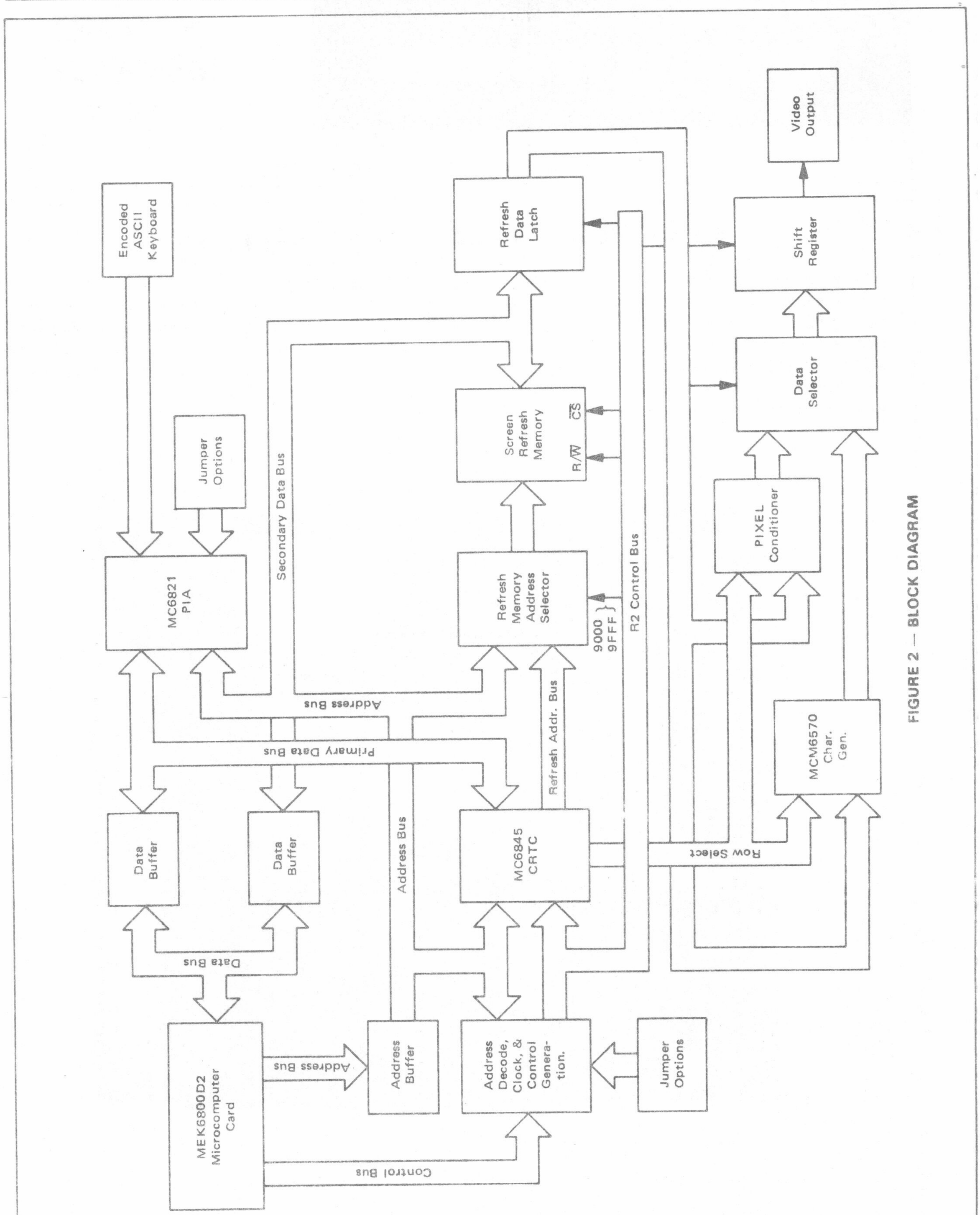



FIGURE 2 — BLOCK DIAGRAM

The MEK68R2M is designed for use with the MEK6802D3 or MEK6802D3C card, which has no self-contained serial interface port. Terminal operation can be achieved via the MEK68IO Input/Output module in conjunction with the R2M and D3 or D3C. The MEK68IO has its own bit rate generator which is independent of the MPU clock. It also contains both RS232 and 20 mA current loop interface, as well as provisions for a modem. The only modifications required for terminal operation with this system are two jumper selections — one for baud rate on the I/O board and the terminal select jumper on the MEK68R2M module.

With either the MEK68R2 or MEK68R2M, the firmware provided contains the necessary intialization procedures for the serial port. These procedures are implemented only if the terminal select jumper is inserted in the R2/R2M card — eliminating any conflict if the serial port is to be used for another purpose.

## CRTBUG OPERATION

The monitor ROM used with the MEK6800R2 is designed to simplify program development. When used with the MEK6800D2, this monitor replaces JBUG. Unlike JBUG, it is a highly subroutined program, allowing the user more freedom in utilizing CRTBUG routines in his own program. As with JBUG, a fully commented source listing is supplied with CRTBUG.

## MEMORY CONTROL

There are a total of six commands which use and/or directly affect memory — including Punch and Load to/from audio cassette. A description of the commands is contained in the following paragraphs.

**Memory Examine and Change.** Any location in memory may be examined with this command. Any location capable of accepting a Write command (RAM, I/O, etc.) may be changed under user control by this command. Sequential locations in either direction may be automatically opened via Line Feed or Backspace. The command is terminated by a carriage return.

**Examine Memory Block.** Starting with the user defined beginning address, eight successive memory locations are displayed in both hexadecimal and ASCII equivalent formats. (If the data is not an ASCII character, a period is displayed.) Sequential blocks may be opened via striking any key other than Carriage Return.

**Op Code Listing of Memory Contents.** Starting with the user defined beginning address, the screen is filled with memory contents arranged in a format of Address, Op Code, Operand, Next Line. The operation can be continued after the screen is full by striking any key other than Carriage Return.

**Fill Memory Block with Constant.** The user defines the starting and ending address of a memory block, and the constant to be used, via the keyboard. The system stores the constant in every location from beginning through ending address.

**Load Memory from Audio Cassette.** Sequential memory locations are filled with data from the audio cassette. The beginning address is that specified by the header on the tape. Data entered is also displayed on the CRT.

**Punch Memory to Audio Cassette.** The user defines the starting and ending address of the memory block to be saved on tape. The system provides the proper header and format. As data is transferred to the tape, it is also displayed on the CRT.

**Register Display.** The contents of the MPU register are displayed in the format:

| C C | B | A | X | P | S |
|---|---|---|---|---|---|
| d d | d d | d d | d d d d | d d d d | d d d d |

The contents of the registers can be changed by using the Memory Examine and Change command. The procedure involves following this command with the displayed value of the stack pointer, then striking Line Feed. The condition code contents will be displayed and may be changed. A line feed then causes the B Accumulator to be displayed. The process is repeated to change any or all registers in sequence except the stack pointer. This register is changed by modifying the data in locations $A008 (most significant byte) and $A009.

## EXECUTION COMMANDS

There are seven commands which initiate execution of a user program. One of these continues program execution from the present program counter location until it is aborted by a breakpoint or Reset. Two others also start at the present program counter location, but execute only one (Trace Next Instruction) or a user specified number (Trace N Instructions) of instructions. These trace commands display the register contents after each instruction.

The remaining four execution commands cause the program counter to be loaded with a user defined starting location, with execution to begin at that point. (Execution continues until aborted by a breakpoint or Reset.) One of these commands requires the user to enter the starting location (via the keyboard) immediately following the command. The remaining three assume the user has previously entered the starting location in one of three specified locations in the "stack" memory. As an example, an exclamation point (!) entry via the keyboard causes the program counter to be loaded with the data in $A00C/$A00D. Execution will start at that point.

## BREAKPOINT CONTROL

Up to eight breakpoints may be entered via the Set Breakpoint at user specified location command. The breakpoint locations are displayed by a Display Breakpoints command. Breakpoints may be cleared individually (Reset Breakpoint at user specified location command) or collectively (Delete All Breakpoints command).

Program execution is suspended when a breakpoint is encountered. The register contents are displayed on the screen, followed by an asterisk (*) on the next line.

## OFFSET CALCULATION

As an aid in utilization of branch instructions, the system calculates offsets on command. The user defines the branch address and the destination address. The system displays a two-byte hexadecimal value. If the branch is in range, the value in the rightmost byte indicates the correct offset. If the branch is out of range, an error message, "Too Far", is displayed, and the leftmost byte indicates the magnitude of the overrange.

## POWER REQUIREMENTS

The MEK68R2 requires a single +5.0 V ± 5% power supply capable of providing 1.1 Adc. This is a maximum value, assuming a RAM population of 1K byte and separate supplies for the keyboard and modulator.

Provisions are made for generating a negative 5.0 V supply for operation of the keyboard. If the required components are added for this feature, a negative 12 Vdc supply capable of providing 125 mAdc is required. For convenience, +12 V, +5.0 V, and –12 V terminations are provided at the keyboard interface socket (U39). The video interface socket (U40) also provides +5.0 Vdc at pin 16.

## OPERATING PRINCIPLES

The MEK68R2/MEK68R2M is controlled by an M6800 family microprocessor operating in conjunction with a monitor ROM such as CRTBUG (supplied with the MEK68R2) or D3BUG2 (supplied with the MEK68R2M). With either ROM, the initiation of the system includes routines which examine the jumper options via Port A of the MC6821 located on the R2/R2M video interface board. This information is then utilized to initialize the MC6845 CRT Controller to the desired format.

As can be seen in the block diagram of Figure 2, the Refresh Memory Address Selector allows the Screen Refresh Memory to be accessed by either the MC6845 or the Microcomputer Unit. In operation, the Address Decode circuitry supplies the control signal for the Address Selector. Thus, an MPU-generated address of 9000 through 9FFF (HEX) allows access by the microprocessor. At all other times, the MC6845 supplies the address for the Screen Refresh RAM.

During initialization, the memory is set up to display an appropriate heading, followed by a cursor. (The remainder of the screen is blanked.) Initialization also involves setting up Port B of the MC6821 to receive data from an ASCII encoded keyboard. This includes using one bit of the jumper option information previously obtained to allow either a positive or negative strobe from the keyboard to be recognized.

Activation of a key causes data to be entered into Port B of the MC6821, and an Interrupt Request to be generated. The microcomputer services this interrupt by reading the B Data Register of the PIA, and temporarily storing this information in memory. The MC6845 is then accessed to determine the cursor location. The microcomputer retrieves the keyboard data from its temporary storage location, then stores it in the cursor location of the Screen Refresh Memory. The screen is automatically blanked during the microcomputer access of the Screen Refresh Memory. The procedure also results in the cursor location being updated.

With the exception of the time period associated with keyboard entry, the Screen Refresh Memory is controlled by the MC6845 and the R2/R2M control bus. Data from the memory is synchronously transferred to the Refresh Data Latch. So long as the most significant bit of this data is zero (indicating ASCII data), it is converted to an appropriate bit pattern by the MCM6670 Character Generator, then loaded into a shift register. This shift register, acting as a parallel to serial converter, drives the video output circuitry.

If bit 7 of the data from the Refresh Data Latch is a logic one, the data is routed via pixel conditioning circuitry to the shift register. This circuitry examines bit 6 to determined the brightness of the character block. The remaining six bits are used to select one of the pixels of the character block. When used in conjunction with the 80 character by 20 line display mode, the graphics mode consists of 60 rows of 160 pixels. (Each pixel consists of a 2-wide by 4-high dot pattern.)

**FIGURE 3a — BITS CONTROLLING VARIOUS PIXEL POSITIONS WITHIN A CHARACTER BLOCK**

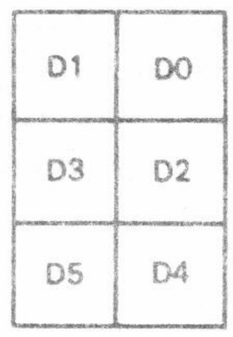
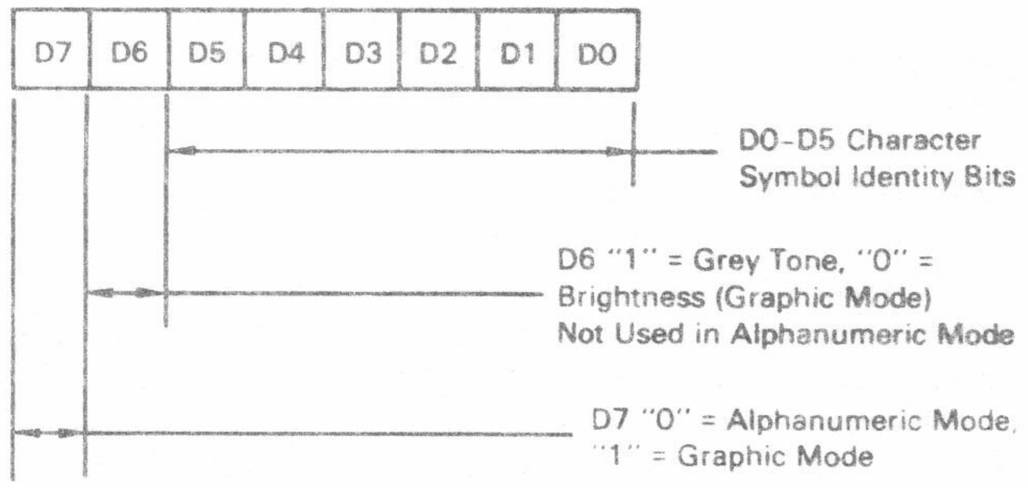



**FIGURE 3b — FORMAT OF CHARACTER DATA**




## SCREEN REFRESH MEMORY

The MEK68R2/MEK68R2M is supplied with two 1024 × 4 RAMs for Screen Refresh. This allows one page of information to be retained when the 65 character by 16 line format is chosen (two pages of 32 × 16 format). Additional RAM sockets are available to allow expansion (up to 4K × 8) for additional character storage or use with other formats. MCM2114 RAMs are recommended for Screen Refresh Memory expansion.

## TERMINAL OPTION

The MEK68R2 can be used in conjunction with MEK6800D2 as a terminal conforming to standard asynchronous data communication formats. In this mode, the MC6850 contained on the MEK 6800D2 is used as the serial port. The modifications required include changing one jumper on the MEK68R2, disconnecting the keyboard/display unit from the D2 kit, and shorting pins 17 and 19 of J2 on the MEK6800D2 microcomputer module. This last modification supplies a 4800 Hz signal as the Receive Clock for the MC6850. This corresponds to a 300 baud transmission rate in the ÷16 mode. Higher baud rates can be achieved by tapping off other outputs of the MC14040 on the D2 MPU board. RS232 interface circuitry can be added in the D2 wirewrap area if required.

## USER INTERRUPT VECTORING

When operating in the monitor mode, interrupt vectors are obtained from memory locations $FFF8–$FFFD. The system allows the use to specify interrupt vectors for user programs by entering data into locations $A000/$A001 (IRQ), $A006/$A007 (NMI), and $A00A/$A00B (SWI). User definition of an IRQ vector does not affect monitor operation. User NMI vector definition renders the trace commands inoperative; user SWI vector definition prevents use of both trace and breakpoints.

## CRT SCREEN/CURSOR CONTROL

The system includes commands to blank the screen and three separate controls for the cursor. These include Enable/Disable, Blink/Non-Blink, and Underline/Non-Underline.

## D3BUG2 COMMANDS

D3BUG2 is the auxiliary monitor ROM supplied with the MEK68R2M for use with the MEK6802D3. It cannot be used with the MEK6800D2 without extensive rework of the D2 kit. In general, it has the same repertoire of commands as found in CRTBUG. Exceptions are that D3BUG2 does not execute "Fill Memory Block with Constant", nor does it perform "Op Code Listing of Memory Contents". D3BUG2 does include more extensive Screen Cursor Control. These functions are:

**Cursor Control/Screen Size.** This command allows the screen size to be defined by the user. The cursor will then automatically proceed to the next line (or page) when the screen border is reached.

**Scroll Page.** Move data page up or down on screen.

**Test Memory Size/Page Boundary.** Allows user to insure that adequate memory is available prior to initiation of new page.

Other commands uniquely available in D3BUG2 (which do not pertain to the screen/cursor control) are:

**Display and Change ROM/RAM pages.** The MC6802D3 allows up to eight pages of ROM and eight pages of RAM to be selected. The D3BUG2 command allows the Page Register on the D3 to be displayed and/or changed without reverting to the Memory Examine and Change commands.

**Punch/Load Tape at 1200 Baud.** The format used is modified KC Standard. Both an MEK6802D3 and an MEK68IO are required to perform this function.

**Verify Tape versus Memory.** This command allows the user to check easily for errors in the Punch/Load function.

## INTERFACE TO MEK6800D2

The MEK6800R2 includes decoding circuitry necessary to generate the I/O 1 and I/O 2 signals utilized by other products in the D3 family. This circuitry is unnecessary if the CRT interface is to be used with the MEK6802D3 It is therefore not included on the MEK6800R2M.

Another signal generated by the R2 and not present with the R2M is termed Activate, or ACT. This signal is asserted low by the R2 decoding circuitry at any time the R2 is addressed. This signal appears at pin 29 of the 60-pin connector. Assuming an MC6800AB Adapter Board is used as a backplane, the $\overline{ACT}$ signal appears at pin 23 of the 86-pin connectors used for the D2 microcomputer module. Modification of the D2 as shown in Figure 4 results in disabling the MC75144 decoder (U11) on the D2 board when $\overline{ACT}$ is low. The data buffers (U4 and U5) therefore remain active, allowing access to the MEK6800R2.

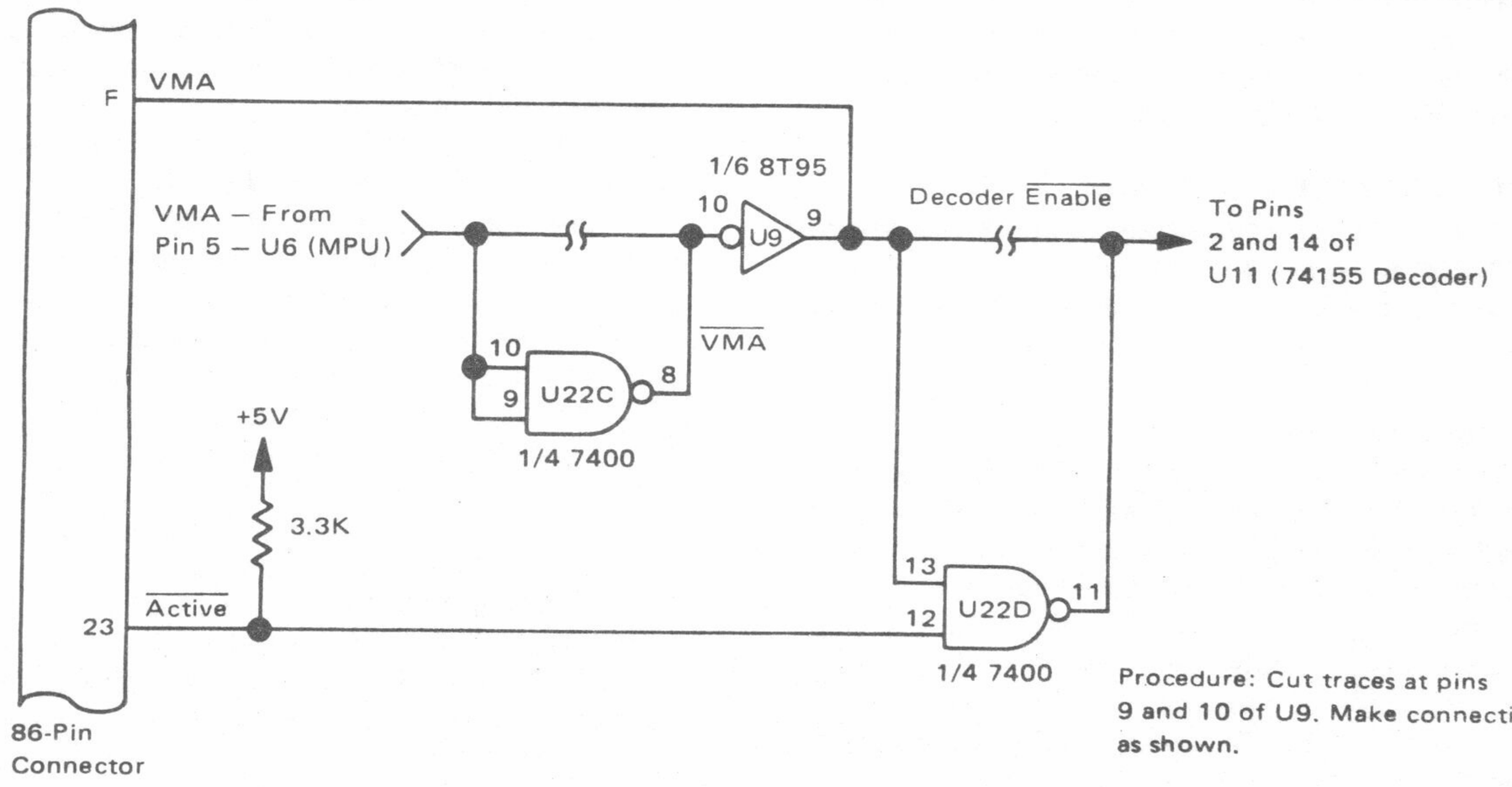
It should be noted that Address Buffers (U1–U3) and Data Buffers (U4 and U5) should be populated with 8T97 and 8T28 buffers, respectively. Either a 7430 or 74LS30 must also be inserted in location U7 on the D2 board to insure operation of the MEK6800R2. If inverting data buffers (8T26) have been previously utilized for U4 and U5, they must be replaced with non-inverting 8T2Bs.

## MEK6800R2 I/O DECODE AND ACTIVATE SIGNALS

The MEK6800D2 and MEK6802D3 microcomputer units differ significantly in regard to address decoding. The latter product provides two signals (I/O 1 and I/O 2) at the bus. These signals, when active, indicate that locations $8000–$80FF or $8100–$81FF, respectively, are being accessed.

Another major difference is that all devices on the MEK6802D3 module are fully decoded. External devices are allowed in any memory location not specifically used by the MPU module. In contrast, the MEK6800D2 allocates specified memory locations which can be used outside the MPU board. For example, an unmodified MEK6800D2 cannot access external memory locations such as $9000–$9FFF even though these locations are not used by the MEK6800D2.

FIGURE 4 — IMPLEMENTATION OF $\overline{\text{ACTIVE}}$



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# MEMORY SYSTEMS

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175 $

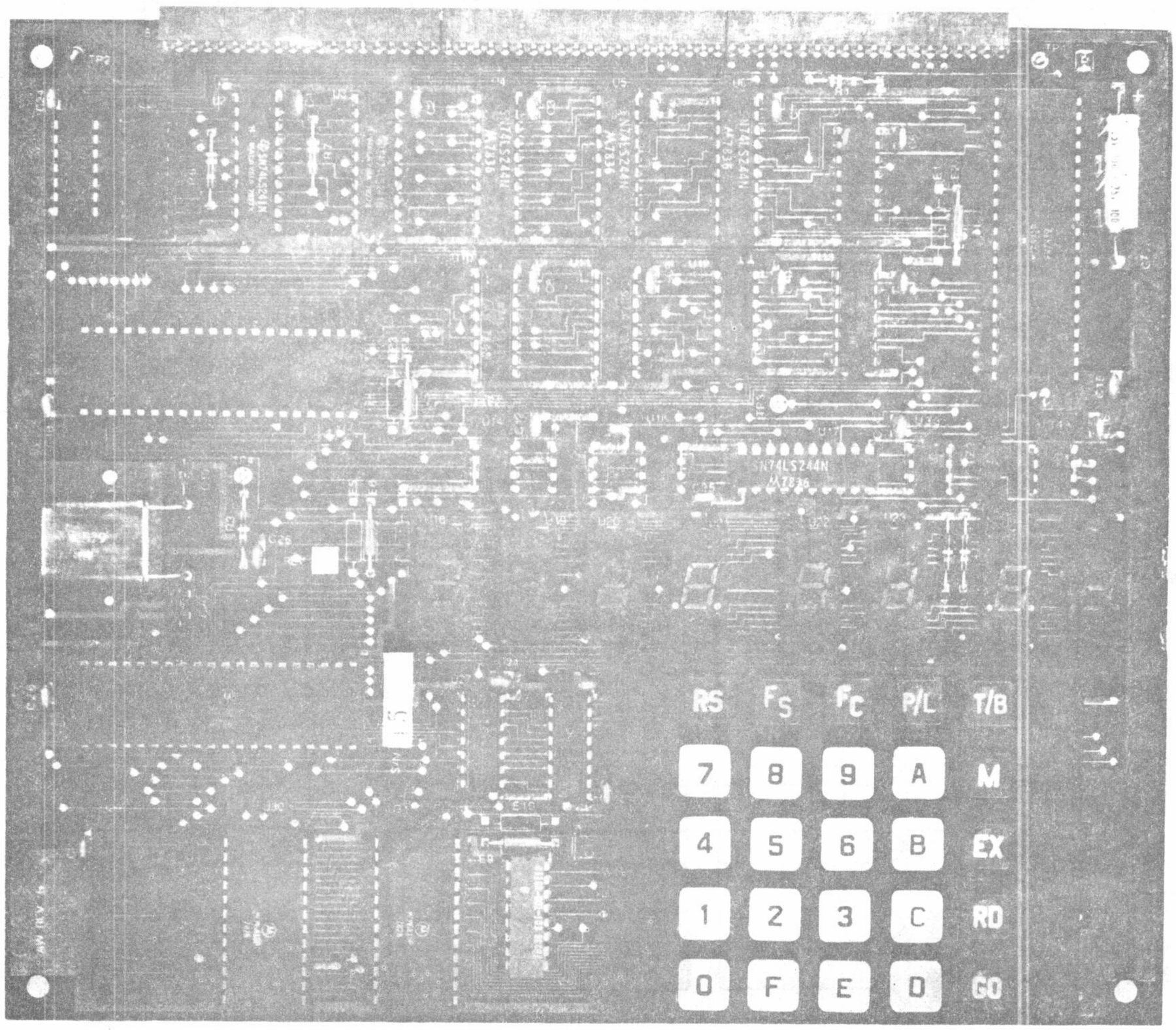
# MEK6802D3
# MEK6802D3C

125 $

## Advance Information

## MICROCOMPUTER MODULE

The MEK6802D3 Microcomputer Module is an Educational/Evaluation product designed to allow the user to become familiar with the MC6802 microprocessor and the MC6846 ROM/RAM/IO/Timer combination. The MEK6802D3 is a self-contained system, utilizing an on-board hexadecimal keypad and LED display user interface. The MEK6802D3C is the same product without the keypad display and associated drivers. Either unit may be used in conjunction with the MOKEP family to form a powerful microcomputer system.




- 2K Monitor Contained in MC6846 Eases Programming Steps
- User Manual (supplied with product) Contains Commented Source Listing of Monitor
- All Bus and I/O Lines Are Buffered
- 256 Bytes of User RAM and 128 Bytes of Stack Included
- Provisions for Expansion ROM Supplied with MEK68R2M (B/W CRT Interface) or MEK68VG (Color TV Monitor Interface)

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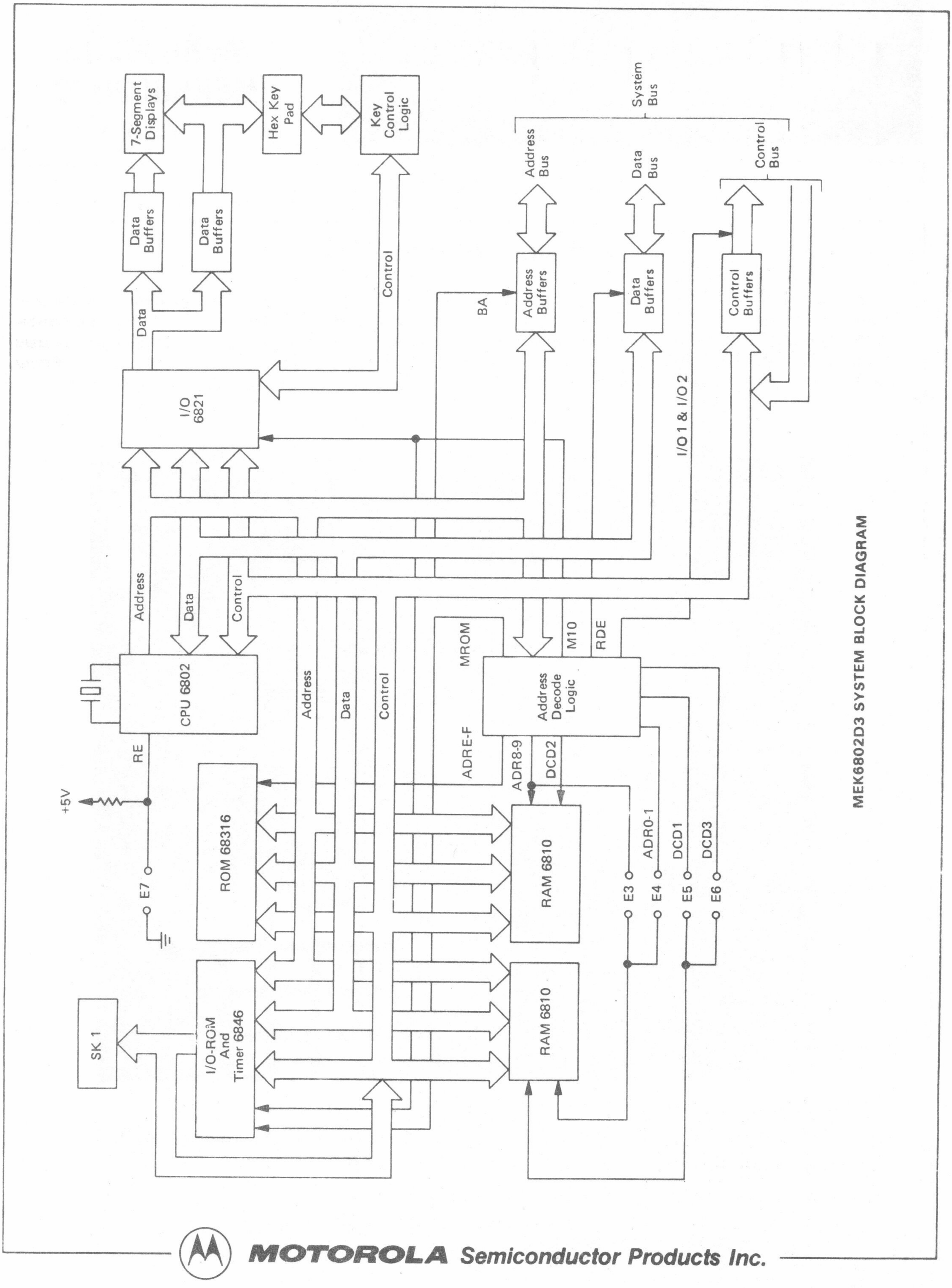
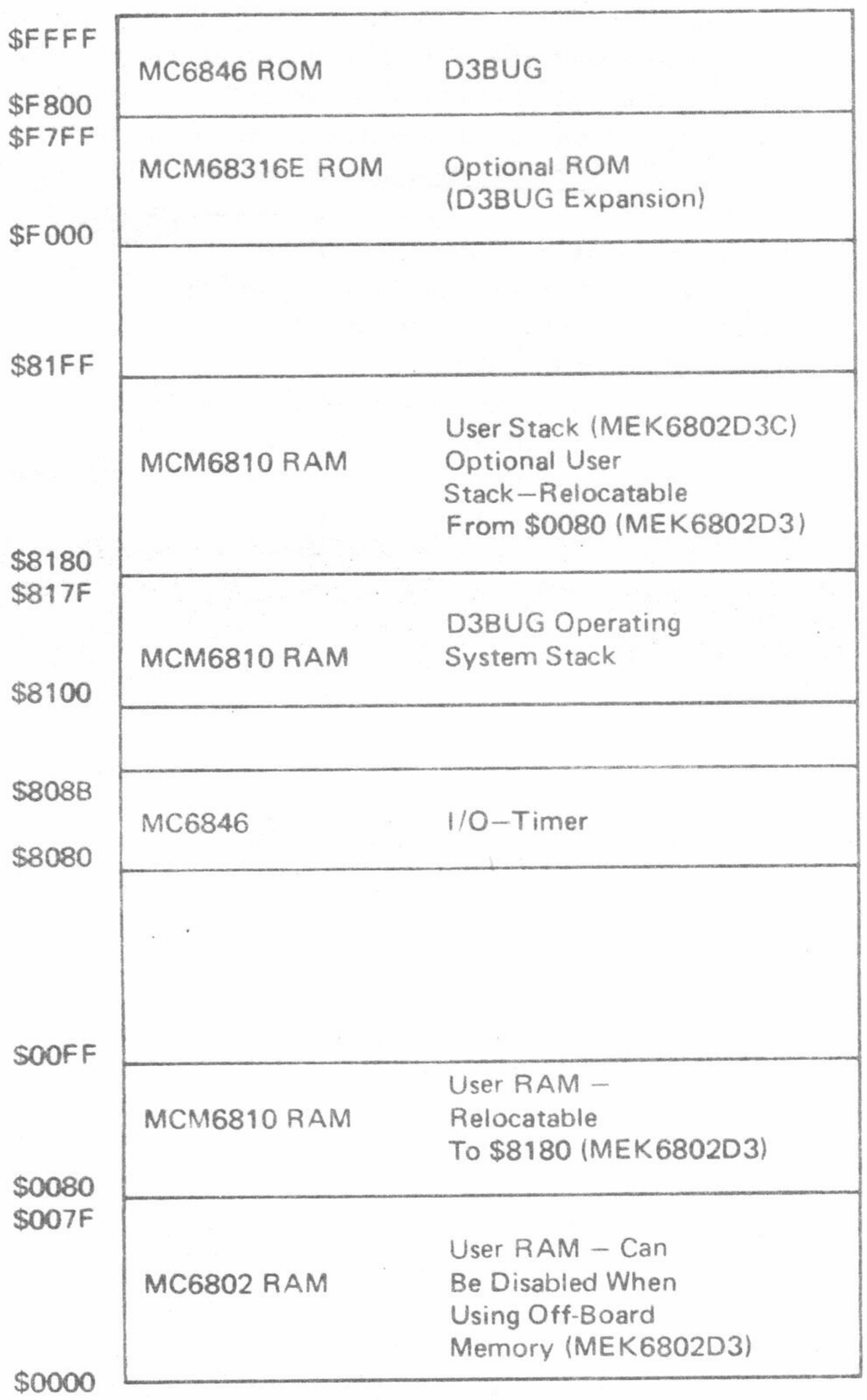



MEK6802D3 SYSTEM BLOCK DIAGRAM

**MEK6802D3 MEMORY MAP**




## MEK6802D3 MICROCOMPUTER MODULE

The MEK6802D3 is designed to function both as a single board microcomputer and as a central processor for an expanded system. The ability to stand alone makes the module an inexpensive tool which is excellent for the learning environment. Everything necessary for a basic system utilizing the 6800 family is located on board. Included are RAM, ROM (containing an expandable operating system monitor), an I/O port, and a keyboard/display unit for developing machine language programs. As need develops for a larger system with increased capability, modules with the required features may be added via the MOKEP family. The MOKEP expansion modules provide many options which enable the MEK6802D3 to become the basis for a complex system.

The MEK6802D3C is designed to function in the expanded system configuration. It has all the features of the MEK6802D3 with the exception of the keyboard/display unit. This module can be used in conjunction with expansion products in systems where a keyboard interface is not desired.

## MEK6802D3 FEATURES

- 2K D3BUG monitor provides keyboard control of board
- On-board RAM for user programming
- Access to an I/O port and a programmable timer
- Memory expansion capable of up to 256K of RAM and 160K of ROM
- Complete line of expansion modules for system add-ins

## HARDWARE FEATURES

The MEK6802D3 module is based on a two-chip system utilizing the MC6802 microprocessor in conjunction with the MC6846. The MC6802 consists of a 6800 type processor plus an on-chip oscillator circuit and 128 bytes of RAM. A standard color-burst crystal (3.579545 MHz) is used by the processor to generate the 894.8 kHz system clock.

The MC6846 has 2K bytes of mask-programmable ROM, an 8-bit parallel bidirectional I/O port with 2 control lines, and a 16-bit software programmable timer-counter. A 16-pin socket is provided on the board to allow the user to interface to the I/O port and timer. There is one Peripheral Interface Adapter, the MC6821, located on the board. It is dedicated to keyboard/display operation and is not available for user access.

The MC6802 provides 128 bytes of RAM located at $0000 through $007F. One on-board MCM6810 provides 128 bytes of stack, while a second can be utilized to expand either the user area or the stack. (As supplied, the MEK6802D3 is configured with 256 bytes of user RAM and 128 bytes of stack.)

The primary operating system for the module utilizes the 2K bytes of ROM located in the MCM6846. Provisions are made on the board for a second 2K byte ROM. This is specifically designed to accept the MCM68316E ROM provided with the MEK68R2M CRT Interface module, or the MEK68VG Color Video Interface card. This allows easy expansion to either a color or black-and-white TV monitor.

Provisions are made for multilevel memory paging to allow the system to be expanded to accommodate up to 256K bytes of RAM and 160K bytes of ROM. Decoding signals (I/O 1 and I/O 2) are also provided to drive MOKEP modules such as the MEK68I/O (Input/Output), MEK68R2M (CRT Interface), and MEK68VG (Color Video Interface).

All address, data, and control lines at the 60-pin bus interface are fully buffered. All on-board devices are fully decoded to minimize address space usage. Both of these features contribute to the expandability of the MEK6802D3.

The MEK6802D3 contains an integral hex keypad and display, providing the hardware necessary for communication with the system. The keypad features nine control keys and sixteen hexadecimal character keys. The display consists of eight 7-segment LED digits.

The module is also available without the hex keypad, display, and associated driver circuitry as the MEK6802D3C. In this configuration, the product is supplied with an MC6808 MPU (equivalent to an MC6802 without RAM). Both MCM6810s are relegated to the stack in the MEK6802D3C version.

## FIRMWARE FEATURES

The 2K firmware monitor for the MEK6802D3 microcomputer system, D3BUG, resides in the MC6846 ROM. The function of the monitor is to provide a means for communication with and control of the system microprocessor by using the keyboard and display. Included in the capabilities of D3BUG are the following features:

1. Examine and change memory locations with ability to increment to next location or decrement to previous location.
2. Automatically verify memory change by displaying both the digits entered and the actual contents of memory.
3. Display and change MPU registers.
4. Calculate offsets for branch instructions.
5. Single step trace of programs in both RAM and ROM.
6. Set, clear, and examine up to 8 breakpoints.
7. Punch designated memory to audio cassette using the MEK68I/O module at either 300 or 1200 baud rate.
8. Load cassette tape into memory.
9. Verify tape after punching or loading.
10. Go to and execute user program.
11. Abort user program.
12. Execute any keyboard control functions during execution of user program.
13. User definition of each of the hexadecimal keys to correspond to a user program.
14. Optional user definition of interrupt vectors.
15. Access to monitor subroutines for user programs.

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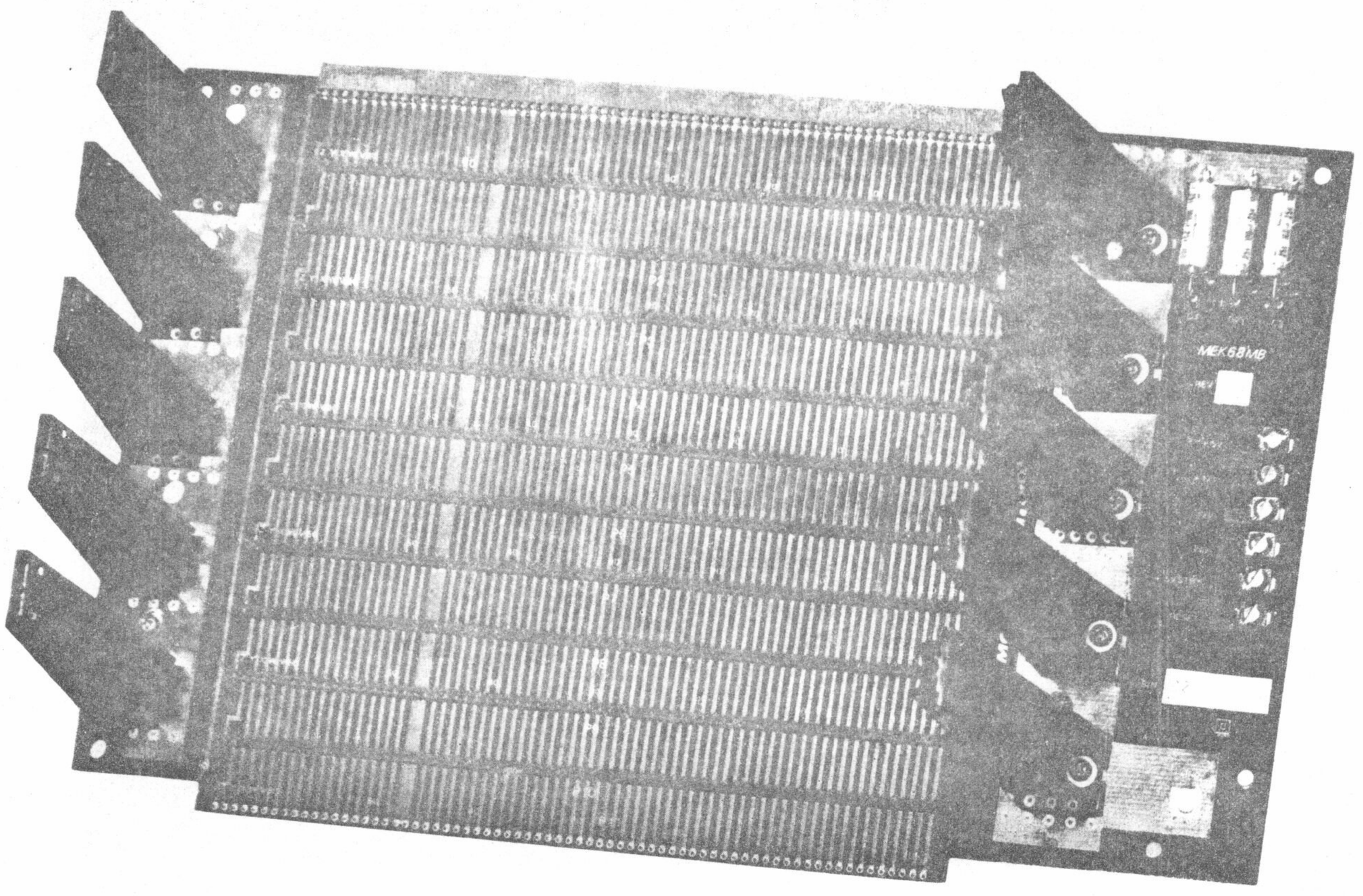
# MEK68MB5

## Advance Information

### MOTHERBOARD

The MEK68MB5 Motherboard Module is designed to be used with other products in the MOKEP (Motorola Kit Expansion Products) family to form a powerful microcomputer system. The MEK68MB5 has provisions for ten slots on 5/8" centers, with alternate slots populated with 70-pin connectors. Provisions for male and female right angle connectors are made at each end to allow for expansion. The Motherboard is supplied with five sets of stand-alone card guides.




- 70-Pin Connectors are Compatible with All 60- and 70-Pin MOKEP Modules
- 0.90" Thick Epoxy G-10 Material with Aluminum Board Stiffeners
- Terminal Block for Power Supply Connections
- Can be Converted to 10-Card Capacity with MEK68CC

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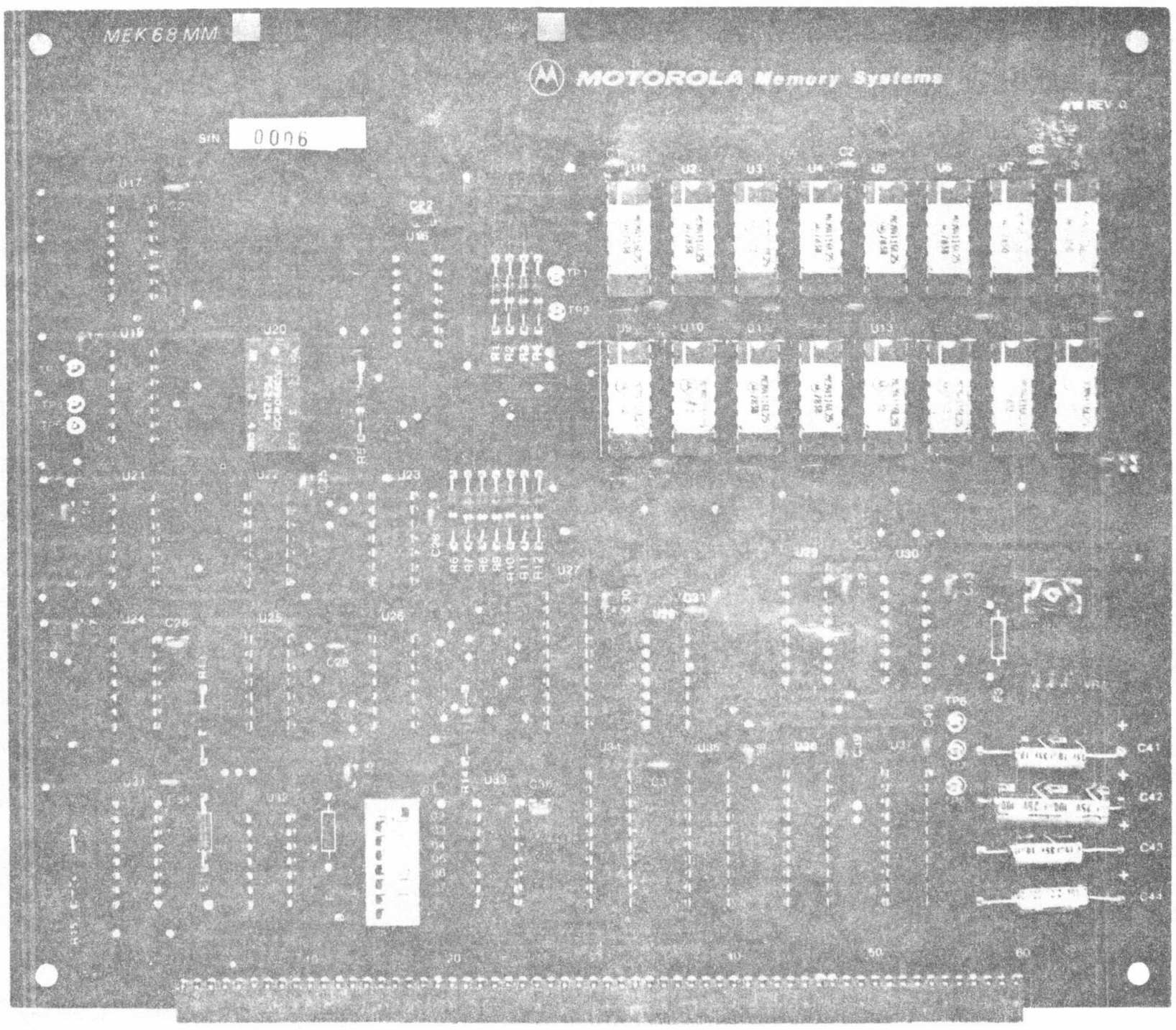
375 $
**MEK68MM32**
**MEK68MM16**
275 $

# Advance Information

## MEMORY MODULE

The MEK68MM Memory Module is designed to be used in conjunction with other products in the MOKEP (Motorola Kit Expansion Products) family to form a powerful microcomputer system. The MEK68MM utilizes a hidden refresh technique to achieve the low cost and minimum power consumption of dynamic memory systems, while appearing as static memory to the system. The MEK68MM fully supports the RAM paging technique of the MEK6802D3 microcomputer module, allowing up to 256K bytes of RAM to be used in the system.




- Hidden Refresh — Memory Appears Static to the System
- Available in 32K Byte (MEK68MM32) and 16K Byte (MEK68MM16) Versions
- Low Cost/Low Power Dissipation
- Capable of Operation in Page Mode Configuration

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# MEMORY SYSTEMS

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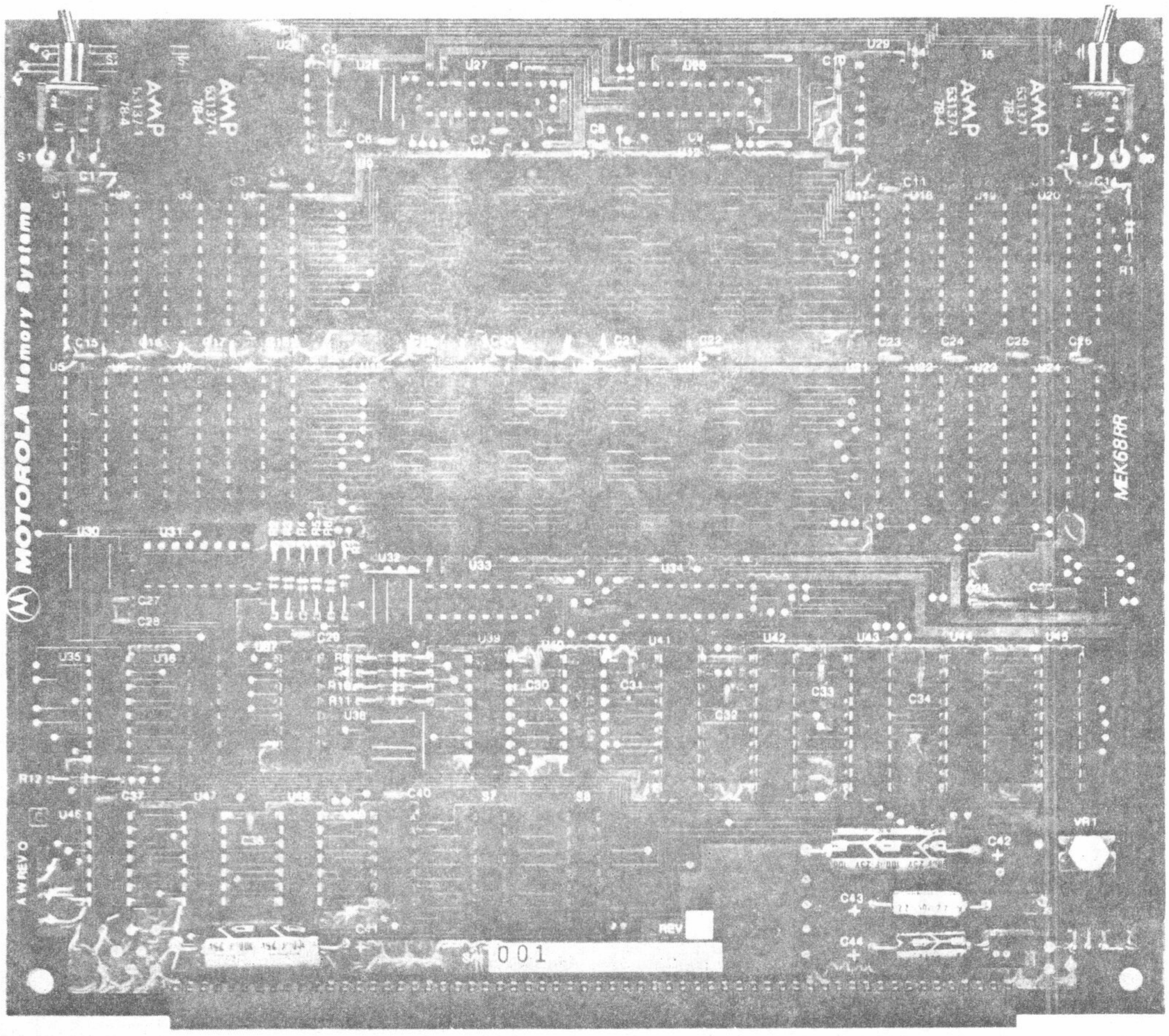
**MEK68RR**

## Advance Information

## ROM/RAM MODULE

The MEK68RR ROM/RAM Module is designed to be used in conjunction with other products in the MOKEP (Motorola Kit Expansion Products) family to form a powerful microcomputer system. The module has provisions for eight ROM sockets and up to 8K bytes of static RAM.




- Two ROM Arrays of Four Sockets Each
- ROM Sockets Accept 1K, 2K, or 4K EPROM or 1K, 2K, 4K, or 8K ROM
- Sixteen RAM Sockets Accept MCM2114 Static RAM
- Two MCM2114s Installed at Factory

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# MEMORY SYSTEMS

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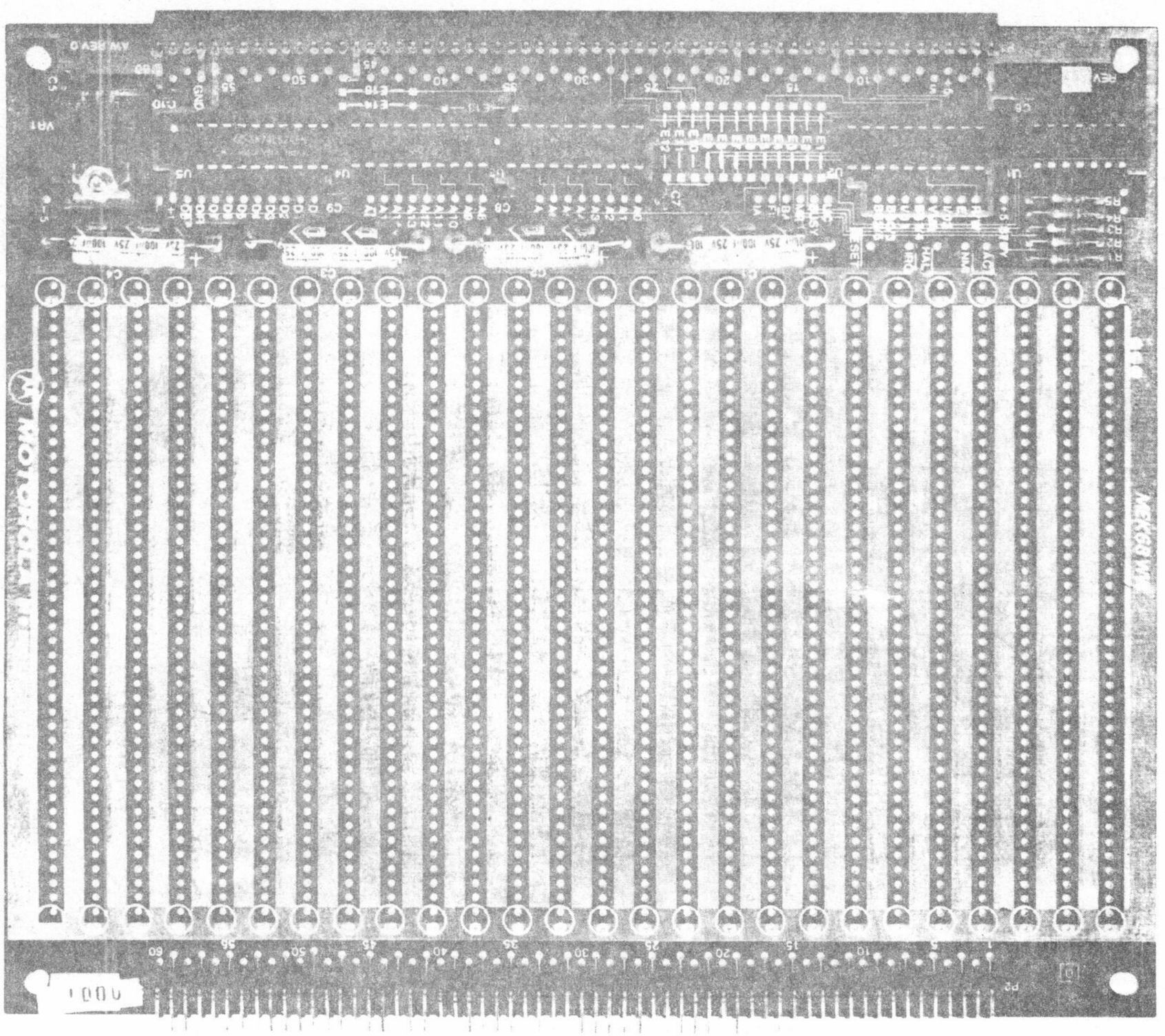
# MEK68WW
# MEK68WW1

## Advance Information

### WIREWRAP MODEL

The MEK68WW/WW1 Wirewrap Modules are designed to be used in conjunction with other products in the MOKEP (Motorola Kit Expansion Products) family to form a powerful microcomputer system. The MEK68WW is intended for use with the MEK6800AB Adapter/Motherboard, and interfaces directly with the 60-pin bus of the AB. The MEK68WW1 utilizes a 70-pin bus, directly interfacing with the MEK68MB series motherboards. Either product can be used as a card extender. Both are supplied with components required for buffering of address, data, and control buses.



- Supplied in Kit (unassembled) Form
- Choice of 60- or 70-Pin Bus Configuration
- 26 Columns (0.3" spacing), Each Having 42 Holes (0.1" spacing)

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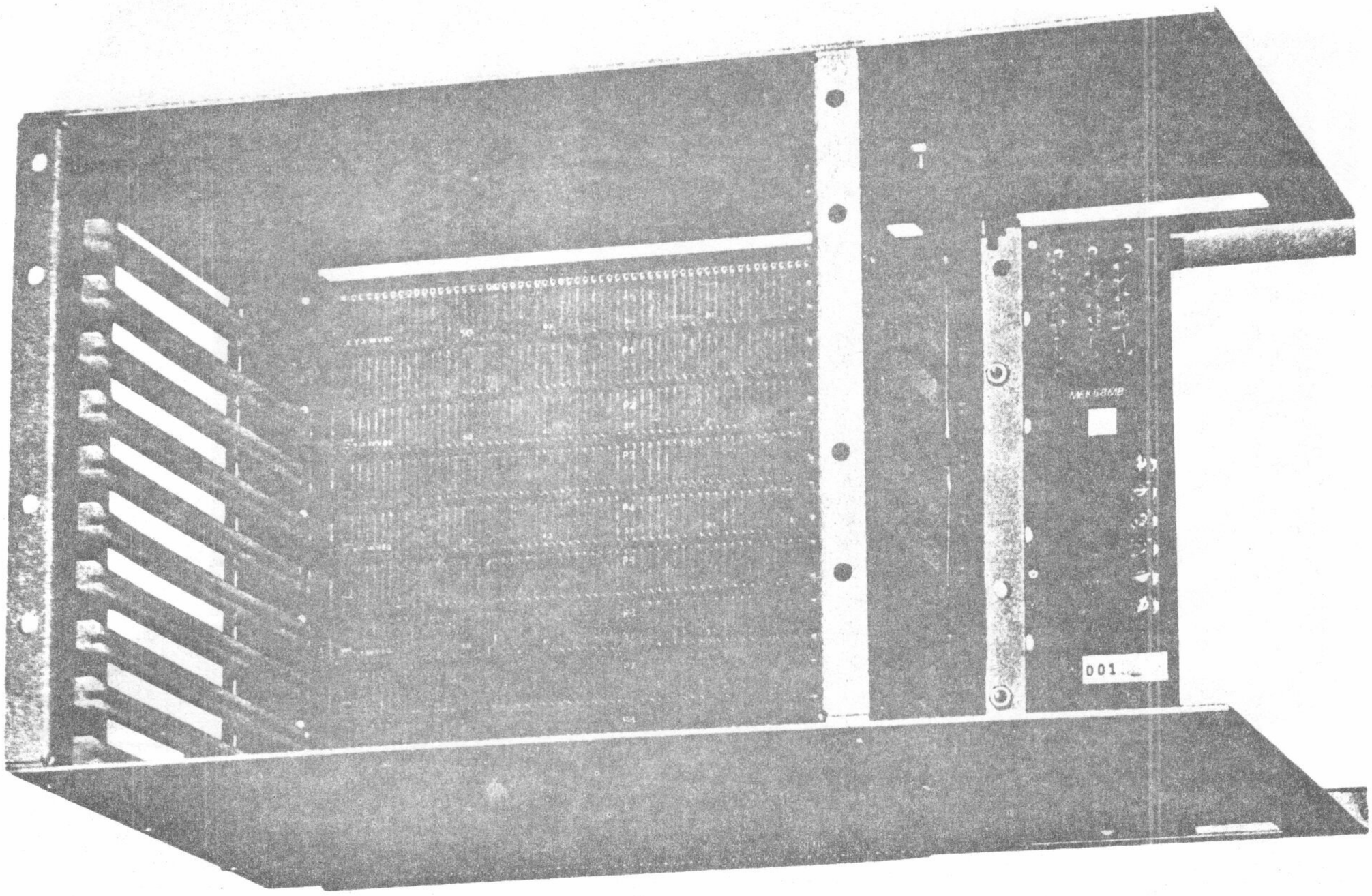
# MEK68CC

## Advance Information

### CARD CAGE

The MEK68CC Card Cage is designed for use with the MEK68MB5 Motherboard. It features all aluminum construction (except for fasteners) and is easily assembled. The Card Cage is supplied with connectors required to convert the MEK68MB5 to 10-card capacity. A full set of 10 card guides is included.




Card Cage shown with Motherboard Installed.

- Dimensions of 8¼" High x 7¼" Wide x 13¼" Deep Allow Mounting in One-Half of Standard 19" Rack Mount Enclosure
- Designed for Convection or Forced Air Cooling

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9.5

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# MEMORY SYSTEMS

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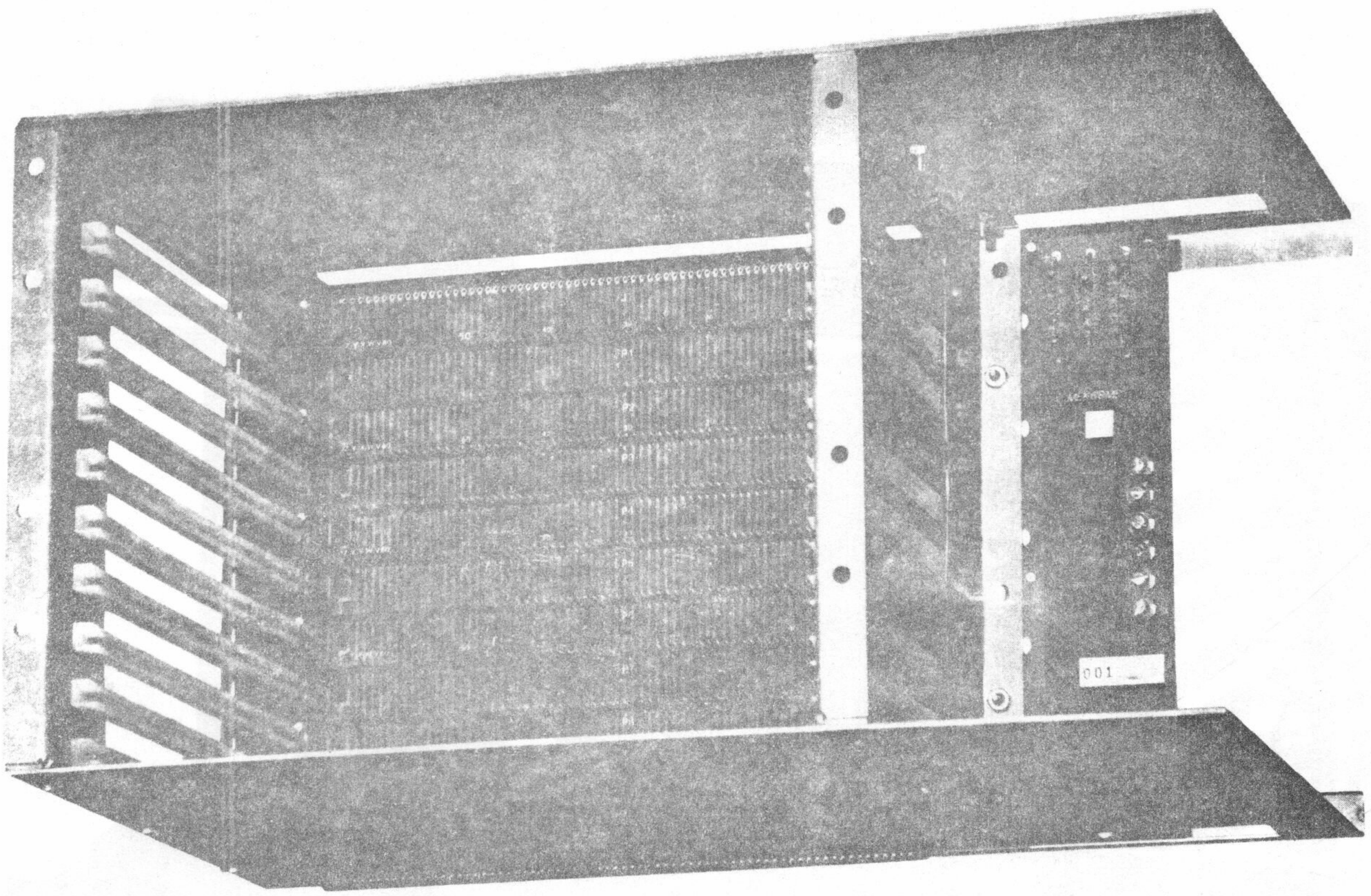
# MEK68CMB

## Advance Information

## COMBINATION CARD CAGE AND MOTHERBOARD

The MEK68CMB Combination Card Cage and Motherboard is designed to house up to 10 cards of the MOKEP (Motorola Kit Expansion Products) family. The card cage is identical to the MEK68CC. The Motherboard is a fully populated version of the MEK68MB5 without the stand-alone card guides. The completed assembly measures 8-1/4″ high × 7-1/4″ wide × 13-1/4″ deep.




- Motherboard Utilizes 70-Pin Connectors — Compatible with All 60- and 70-Pin MOKEP Modules
- Motherboard Is Constructed of 0.90″ Thick Epoxy G-10 Material
- Terminal Block on Motherboard for Power Supply Connections
- Mounts in One-Half of Standard 19″ Mount Enclosure
- Designed for Convection or Forced Air Cooling

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